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PAPER

Fabrication of surface ion traps with integrated current carrying wires enabling high magnetic field gradients

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Abstract

A major challenge for quantum computers is the scalable simultaneous execution of quantum gates. One approach to address this in trapped ion quantum computers is the implementation of quantum gates based on static magnetic field gradients and global microwave fields. In this paper, we present the fabrication of surface ion traps with integrated copper current carrying wires embedded inside the substrate below the ion trap electrodes, capable of generating high magnetic field gradients. The copper layer's measured sheet resistance of 1.12 mΩ/sq at room temperature is sufficiently low to incorporate complex designs, without excessive power dissipation at high currents causing a thermal runaway. At a temperature of 40 K the sheet resistance drops to 20.9 $\mu\Omega$/sq giving a lower limit for the residual resistance ratio of 100. Continuous currents of 13 A can be applied, resulting in a simulated magnetic field gradient of 144 T m^{-1} at the ion position, which is 125 μm from the trap surface for the particular anti-parallel wire pair in our design.

1. Introduction

Since the first quantum gates using trapped ions were proposed by Cirac and Zoller [1], trapped ions have been considered to be a promising qubit platform to realise large-scale quantum information processing. Experiments have proven the capabilities of trapped ions to be used as physical qubits, including high-fidelity state preparation [2–4], universal gate operation [4–6] and readout [4, 7], and long coherence times [4, 8, 9]. In addition to these experiments using single ion strings, there has also been research into expanding the ion trapping system into a large scale architecture, and increasing the number of qubits that can be processed in parallel and entangled for implementation of more complex quantum algorithms [10, 11]. The key of this research, inspired by the proposals of Wineland *et al* [12] and Kielpinski *et al* [13], is making all macroscopic devices for trapping ions completely scalable. Surface ion traps developed using micro-electro-mechanical system fabrication technology [14–17] and the concept of junction nodes connecting linear ion trapping zones [18–20] have significantly increased the number of ions that can be trapped and controlled on a microchip. Optical and electrical components such as micro-mirrors [21] and optical waveguides [22–25], photodetectors [26–28], digital-to-analogue converters [29], and trench capacitors [30] can be fabricated in microchips and integrated in the same chip together with ion traps.

A major challenge for increasing the number of qubits is the simultaneous large-scale control of quantum gates, and a few methods have been developed for trapped ions. For laser based gates, integrated optical waveguides and gratings [22–25] are a promising approach. As a different approach, laser free high fidelity gates have been demonstrated using oscillating magnetic field gradients [31, 32]. Another approach is to use long-wavelength radiation combined with a static magnetic field gradient as proposed by Mintert

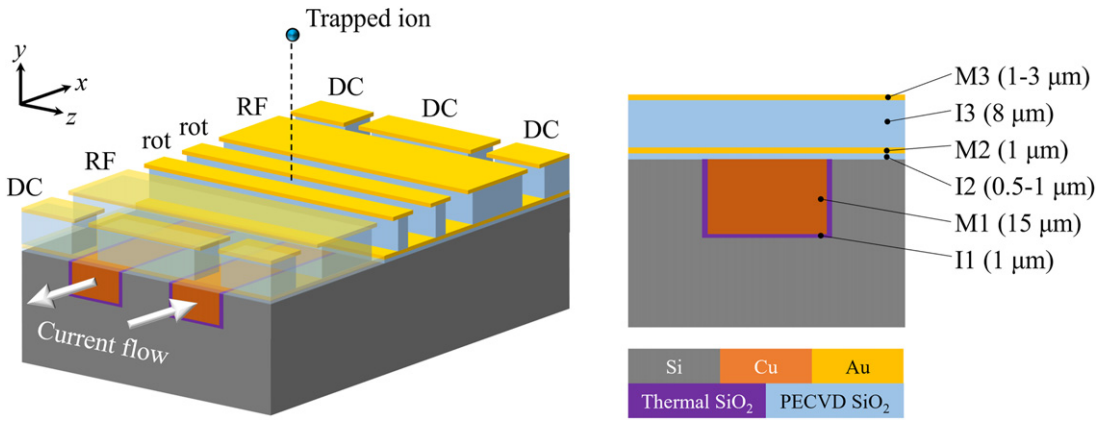

Figure 1. Schematic of the proposed surface ion trap with integrated CCWs (not to scale). A set of segmented DC electrodes and RF electrodes are shown as transparent to show part of the copper wires integrated under the electrodes. The vertical dimensions of the ion trap electrodes and CCWs are shown on the right.

and Wunderlich [33]. Weidt *et al* have further built on this work and demonstrated a quantum computing approach where quantum gates can be executed simply by the application of a semi-static voltage to a microchip making use of locally applied magnetic field gradients, and global microwave and RF fields [34]. Lekitsch *et al* have developed a microchip-based blueprint for a fault-tolerant quantum computer capable of hosting millions of qubits [35]. In the proposed architecture, microfabricated surface ion traps and integrated current-carrying wires (CCWs) are used to trap ions and generate a high static magnetic field gradient in designated gate zones on the chip.

Historically, CCWs have been used extensively for the confinement of neutral atoms, allowing the technology to shift from free-standing wires to more robust microfabricated atom chips [36]. In atom chips, a single layer of evaporated gold up to several micrometres thick is widely used for CCWs [37, 38]. Furthermore, multilayer atom chips have been demonstrated [39], some allowing currents up to 10 A in 15 μm thick CCWs [40], including one featuring 2 μm thick copper CCWs embedded into the silicon [41]. For ion traps with integrated CCWs, the wires need to be combined with a top layer structure capable of applying the required high RF voltages, and dielectrics in sight of the ion should be avoided.

In ion traps with CCWs in the top layer, static axial magnetic field gradients of 2.3–23 T m^{-1} have been demonstrated [42–44]. Oscillating magnetic field gradients of 7, 35 and 55 T m^{-1} in the 1–3.2 GHz range have been reported at ion heights of 75, 30 and 35 μm respectively [45–47], as well as a radial gradient at 5 MHz of 152(15) T m^{-1} at an ion height of 30 μm [32], all with the CCWs located in the top layer of the ion trap. In a different implementation where 127 μm thick copper wires have been placed on a chip carrier below the ion trap, a static magnetic field gradient of 16 T m^{-1} at an ion height of 96.9 μm has been achieved [48].

In our design the CCWs are embedded in the silicon substrate perpendicular to the RF trapping electrodes as shown in figure 1. In this concept, the design of the CCWs is completely independent from the design of the top electrode layer. This removes the constraints that have limited the axial gradient with CCWs in the top layer, without moving the CCWs significantly further away from the ion. With a sufficiently low sheet resistance of the copper for the management of thermal dissipation from the current, high currents in excess of 10 A can be applied allowing magnetic field gradients in the range of 100–150 T m^{-1} at an ion position 125 μm from the trap surface.

In this paper, we present the design and fabrication of surface ion traps with integrated CCWs for high magnetic field gradients. A fabrication process consisting of integration of copper wires in the silicon substrate and fabrication of ion trap electrodes on top of this structure was developed. In order to reduce the effect of stray electric fields induced by built-up charges on dielectric surfaces, gold was used for conducting layers exposed to the ion to avoid native oxide formation, and the thick oxide layer underlying the uppermost metal layer was undercut. Application of high currents up to 13 A continuous, resulting in a simulated magnetic field gradient of 144 T m^{-1} at the ion position of 125 μm, was demonstrated on the fabricated wires, and power dissipation was measured. The fabricated chips were also used to trap $^{171}Yb^{+}$ ions. Considering the gate mechanism, a magnetic field gradient of 100–150 T m^{-1} should enable much stronger sideband transitions and is predicted to give rise to a two-qubit gate fidelity of ~99.9% [34], significantly higher than the fault-tolerant threshold for the surface code [49].

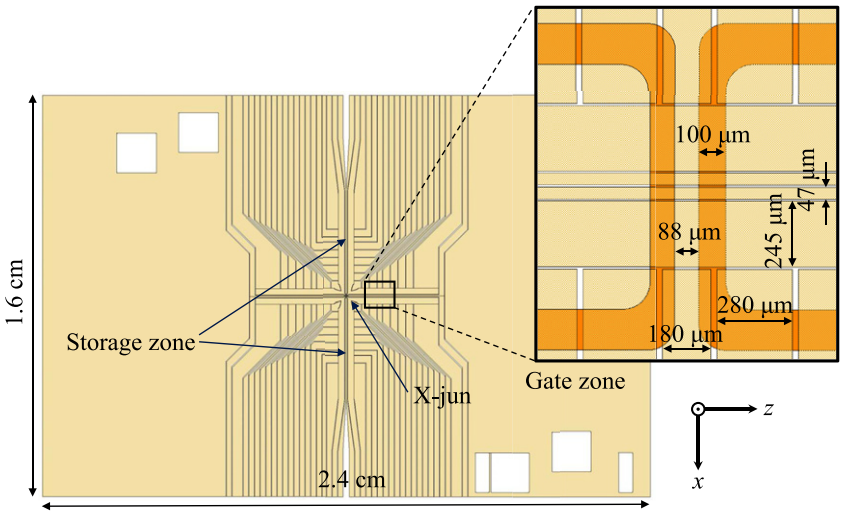

Figure 2. Layout design of ion trap showing the gate zone and storage zones. Ions can be shuttled between zones via the *X*-junction in the centre of the device. The white squares represent the bonding pads for the CCWs. The magnified view shows the electrode and CCW design in the gate zone.

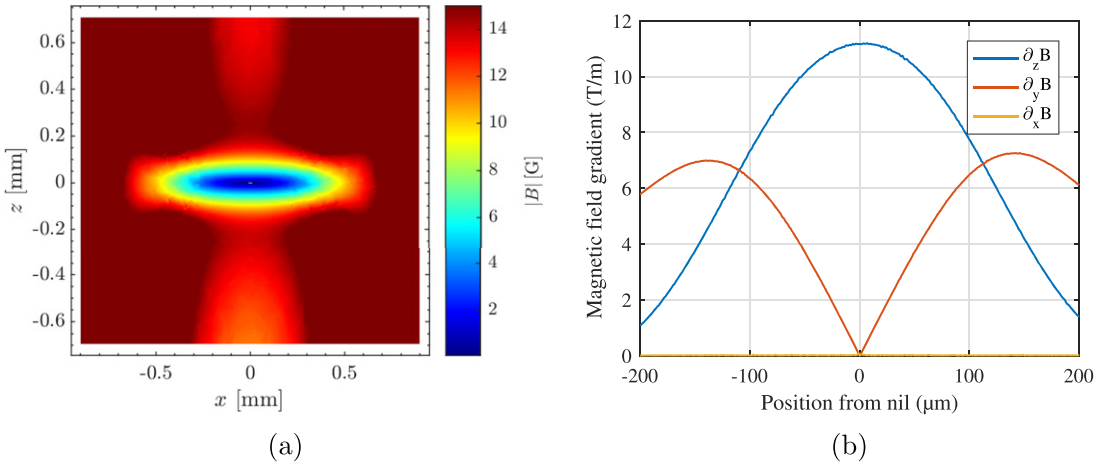

Figure 3. Finite element method simulation results of the CCW structure designed for this experiment per 1 A input current. (a) Magnetic field magnitude $|B|$ in a horizontal plane at the trapping height ($h_{\text{ion}} = 125\ \mu$m) with the magnetic field quadrupole clearly visible in the centre at ($x = 0$; $y = h_{\text{ion}}$; $z = 0$). (b) x-, y-, and z-components of the gradient of the magnetic field magnitude along the axial trapping axis z. Close to the quadrupole centre, the magnetic field gradient ∂B is maximal with a gradient of 11.1 T m^{-1} per 1 A input current. At 13.4 A this gives the 150 T m^{-1} necessary for high fidelity gates proposed by Weidt *et al* [34].

2. Design

The vertical dimensions of the designed ion trap electrodes are shown in figure 1. The thickness of the oxide layer (I3) isolating the top layer (M3) and the ground plane (M2) is 8 μm, where we measured a flashover voltage of over 250 V_{amp} at 15 MHz between the RF electrode and the ground plane using a test structure chip. The ion height numerically simulated by the lateral design of electrodes is 125 μm from the electrode surface. The two central DC electrodes between the RF rails are used to apply compensating DC voltages for principal axis rotation.

The gate zone incorporating the CCWs is located in one of the four arms of the *X*-junction (figure 2). The design of the *X*-junction is adapted from [50]. The trapped ions can be shuttled to two storage zones with a low magnetic field of <2 mT placed in the two perpendicular arms. Two parallel wires are placed perpendicular to the RF rails, and DC currents with opposite directions are applied to the wires to maximise the magnetic field gradient at the ion position. 100 μm, 15 μm, and 88 μm for the width and depth of wires and the distance between the wires respectively were chosen to give a good trade-off between current density and power dissipation, and maximum magnetic field gradient. The gradient is only reduced by 17% compared to the ideal case of two infinitely thin wires located on the silicon surface, while limiting

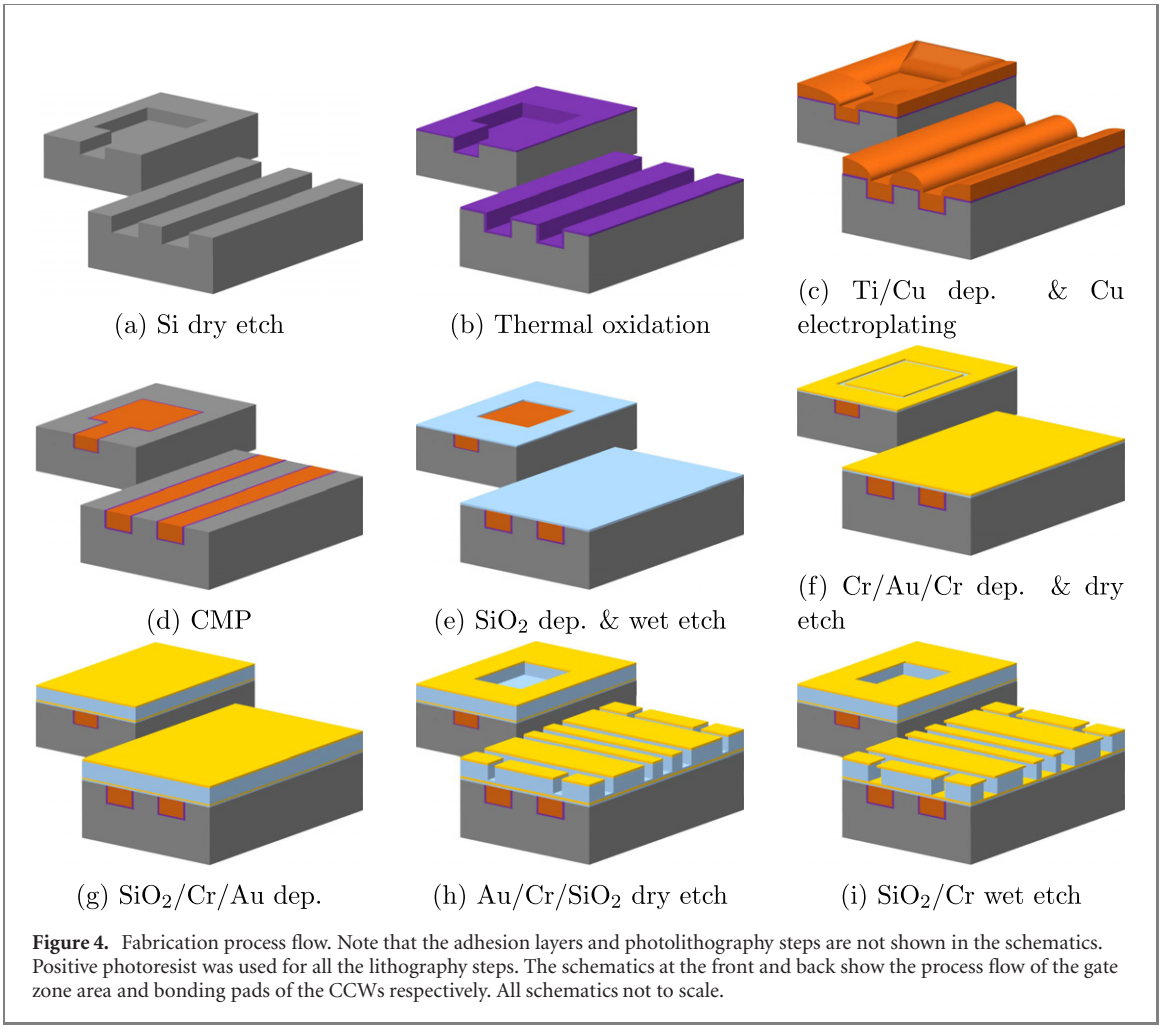

Figure 4. Fabrication process flow. Note that the adhesion layers and photolithography steps are not shown in the schematics. Positive photoresist was used for all the lithography steps. The schematics at the front and back show the process flow of the gate zone area and bonding pads of the CCWs respectively. All schematics not to scale.

the current density to 1×10^6 A cm^{-2} at 15 A. The overall CCW structure corresponds to a wire with a length to width ratio of 390. Finite element method simulation results show that by applying 13.4 A to the wires, a magnetic field gradient of 150 T m^{-1} along the longitudinal trap axis can be generated at the ion position (figure 3). Depending on the precise gate implementation, a gradient in the range of 100–150 T m^{-1} is desirable.

A further consideration for the CCW design is ohmic power loss and substrate heating, mainly determined by the resistance of the wires. The 15 μm thick copper layer has a sheet resistance of 1.12 mΩ/sq at room temperature. This low sheet resistance allows for a resistance at room temperature of 438 mΩ for our CCWs in series, despite the complex design. The resistance is predicted to be reduced to 15.0–49.5 mΩ at the intended operating temperature of 40–70 K, assuming a copper layer with a residual resistance ratio (RRR) of 50. This resistance corresponds to a power dissipation of 2.3 W when applying 10 A assuming a cooling system with a base temperature of 40 K and 5 K W^{-1} overall thermal resistance, which is a conservative estimate for our setup from previous measurements.

3. Fabrication

This section describes the fabrication process of integrating the CCWs into the silicon substrate and building ion trap electrodes on top of the CCW-integrated wafer. First, the CCW layout is photolithographically patterned on the silicon wafer using a conventional deep reactive ion etching process (figure 4(a)). After stripping the used resist followed by a standard RCA clean, the wafers are thermally oxidised in a furnace tube to grow wet oxide of 1 μm, forming an insulating layer between the silicon substrate and the CCW (figure 4(b)). Then, Ti/Cu with a thickness of 10/200 nm is deposited by a sputtering process, and using this as an adhesion and seed layer, a 25 μm-thick copper layer is subsequently electroplated to form the CCWs (figure 4(c)). The fabricated structures are planarised by a three-step sequence that consists of diamond milling and two chemical mechanical polishing steps. Optimising the

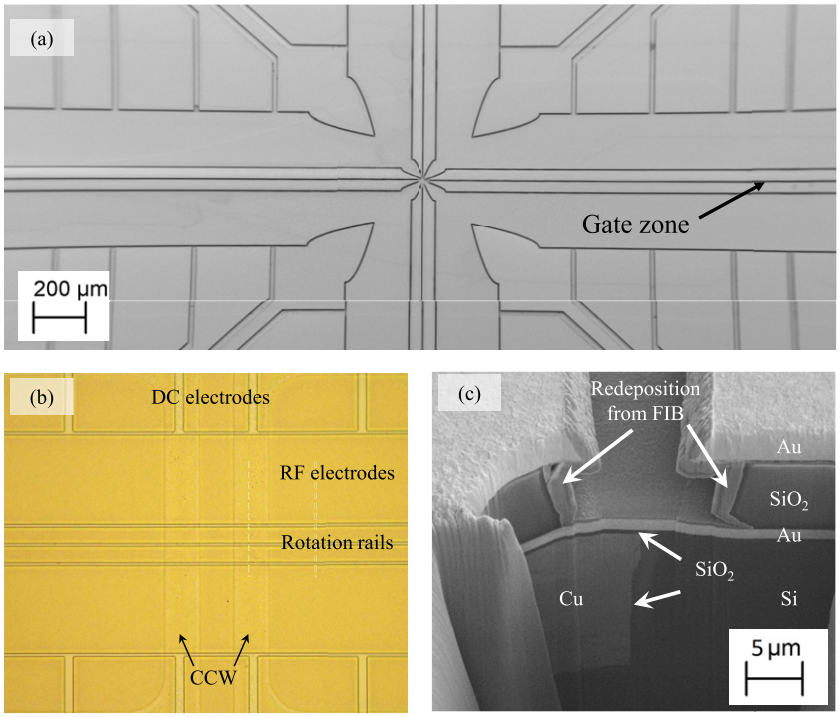

Figure 5. (a) SEM image of the *X*-junction. (b) Optical microscope image of the trap, showing the gate zone. (c) SEM image of the cross-section of the device made by a FIB.

process parameters, a dishing of approximately 100 nm for 100 μm to 1500 μm wide patterns was achieved. This concludes the fabrication of the CCW base wafer (figure 4(d)).

Fabrication of the ion trap electrodes starts with plasma-enhanced chemical vapour deposition of a 0.5–1 μm-thick SiO_2 layer (figure 4(e)). The oxide layer is patterned by wet etching using buffered oxide etchant (BOE) ($HF:NH_4F = 1:7$) to open the bonding pads for the CCWs. Then, a Cr/Au/Cr layer of 10/1000/10 nm is sputtered and ion-beam-etched to provide the ground plane as well as the bonding pads for the CCWs (figure 4(f)). The thin chromium layer is used to increase adhesion between silicon oxide and gold. Next, an 8 μm-thick SiO_2 layer and 10/1000–3000 nm-thick Cr/Au layer are deposited (figure 4(g)). These two layers are dry etched sequentially using the same photoresist mask (figure 4(h)). The good uniformity (4(1)%) of the deep oxide etching process allows stopping 750(250) nm before reaching the Cr/Au/Cr layer, in order not to expose the gold to the oxide etching chemistry. The remaining oxide is etched by BOE based wet etching. This wet etching also etches the sidewalls of the oxide pillar, resulting in the formation of the electrode undercut structure (figure 4(i)). After the BOE, the exposed Cr adhesive layer over the Au ground plane is removed by an additional wet etching process. Finally, a 10/500 nm Cr/Au layer is sputtered on the back of the wafer to improve indium bonding of the traps.

An optical microscope image showing the top view of the gate zone, a scanning electron image (SEM) image of the *X*-junction, and an SEM image of the cross-section of the devices fabricated by a focused ion beam (FIB) are shown in figure 5. The cross-section is placed at the end of the west arm of the *X*-junction where a routing wire of the CCW is parallel to the two rotation electrodes, which are separated by 5 μm. The oxide below the rotation electrodes shows the desired undercut of 3(1) μm from the oxide wet etch. Every surface in the line of sight of the ion beam impact is covered with some redeposited material, which is unavoidable. The resistance between the copper tracks and surrounding conducting layers was higher than our measurement limit (10 MΩ), and no unintended electrical short was observed between ion trap electrodes.

4. Experiments

The resistance of the CCW at room temperature was measured using four-terminal sensing with 100 mA source current. The fabricated CCWs match the expected resistance within <1%. To evaluate performance at low temperatures, the device was mounted in a custom cryogenic system as shown in figure 6. The fabricated trap was indium soldered to a copper block, which extends through a hole in the printed circuit board (PCB) to which it is attached. The CCWs were connected by ten 25 × 125 μm ribbon bonds per pad

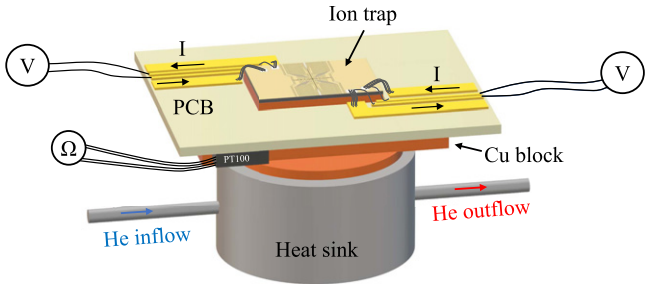

Figure 6. The fabricated trap is bonded to a copper block using indium with a PCB attached. The CCWs are connected by ten 25 × 125 μm aluminium ribbon bonds per pad to a PCB and by one ribbon bond for voltage sensing connections. The temperature is measured using a PT100 attached to the copper block. The copper block is then mounted on a heat sink located in a custom UHV test chamber, which is connected to a custom closed-loop cryogenic helium gas circulation system.

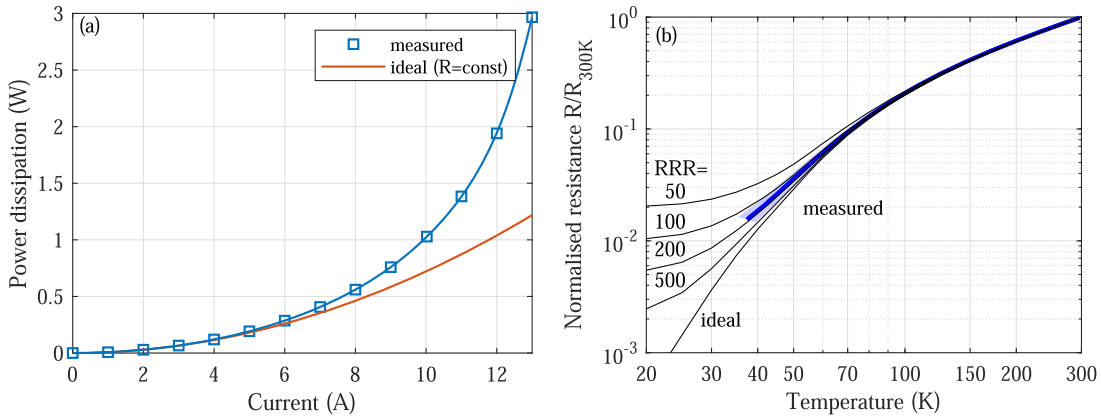

Figure 7. (a) Measured power dissipation over applied current through the whole CCW structure, compared to the ideal case where the trap does not heat up. (b) Normalised resistivity of CCW over temperature. The measured resistance (blue with the uncertainty as shaded area) is compared to copper with different RRR for comparison.

to the PCB and by one ribbon bond for voltage sensing connections. The temperature was measured with a calibrated PT100 (Lakeshore Pt-111-14H) attached to the copper block. The copper block was then mounted on a heat sink (using AuSn preforms in-between) located in a custom ultra high vacuum (UHV) test chamber, which was supplied by a custom closed loop cryostat [51]. The measurements were performed at a pressure of $\sim 10^{-6}$ mbar and a base temperature of 38(2) K.

To characterise the power consumption of the CCWs, current was applied through all CCWs in series, and the voltage drop was directly measured at the CCW pads (via sensing bond wires). At a current of 10 A the power dissipation is 1028(10) mW (figure 7(a)), which is 1.43 times higher than it would be without heating the trap. The rise in resistivity by a factor of 1.43 corresponds to a rise in temperature of the CCWs from 38 K to 43 K, while the temperature measured on the copper block is 40 K. The maximum continuous current of 13 A was limited by thermal runaway which can be improved by optimising the thermal anchoring.

To obtain the temperature dependence of the resistance, the helium flow was turned off and the resistance was measured as the system was heating up (2 K min^{-1}). A probe current of 10 mA was used for the four-terminal sensing of the CCW resistance. At 40(1) K the resistance drops from 438(1) mΩ by a factor of 54(2) to 8.2(4) mΩ and at 70(1) K by a factor of 10.7(1) to 40.8(4) mΩ. This corresponds to a sheet resistance of 20.9(9) $\mu\Omega$/sq at 40(1) K and 104(1) $\mu\Omega$/sq at 70(1) K. Figure 7(b) shows the normalised resistance (blue with uncertainty as shaded area) compared to Cu with an RRR of 50, 100, 200 and 500 and pure Cu (data from [52]). The measurement setup does not allow a precise number for RRR to be obtained, but is estimated as 180^{+215}_{-65} with a lower bound of 100.

Fabricated chips with integrated CCWs were successfully used to trap $^{171}Yb^{+}$ ions as shown in figure 8. We note that the chip used for trapping is slightly modified earlier version of the design described in section 3 featuring an aluminium ground plane instead of a gold ground plane. We had adjusted the fabrication process in order to avoid an aluminium electrode, as such an electrode could potentially form a

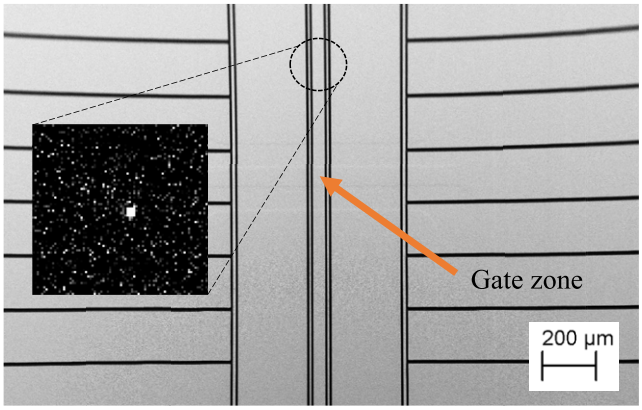

Figure 8. SEM image of the fabricated device. The inlay shows an image of a trapped ion captured by an electron-multiplying charge-coupled device sensor.

very thin oxide layer and charge up. We also replaced the central ground electrode and four thin rotation electrodes by two central DC electrodes for the newer design to enable a simpler principal axis rotation and to enable more undercut of the dielectric below the electrodes. During trapping, we note that we did not observe any adverse effects because of the aluminium ground plane. Ions have been trapped on this device, frequently for 7–16 h.

5. Conclusion and outlook

We have presented the fabrication of surface ion traps with CCWs integrated into the silicon substrate. The dishing of the CCWs is well controlled, with 100 nm for both small features and large features, ensuring the electrical performance is not compromised. The RRR is estimated as 180^{+215}_{-65} with a lower limit of 100 giving a resistance close to that of pure copper at the temperature ranges in our application. These devices are capable of providing high currents of 13 A continuous for high static magnetic field gradients of 144 T m^{-1}, at an ion position of 125 μm from the trap surface. These results indicate that the devices are suitable for high fidelity quantum gates based on static magnetic field gradients and global microwave fields, constituting a promising approach for building practical trapped ion quantum computers with millions of qubits.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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