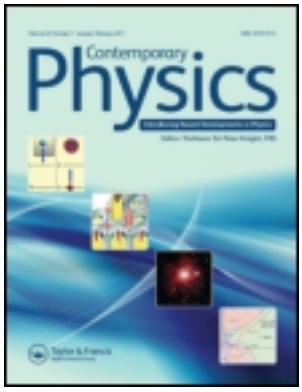
This article was downloaded by: [University of Sussex Library]
On: 09 December 2011, At: 06:23
Publisher: Taylor & Francis
Informa Ltd Registered in England and Wales Registered Number: 1072954 Registered office: Mortimer House, 37-41 Mortimer Street, London W1T 3JH, UK



Contemporary Physics
Publication details, including instructions for authors and subscription information:
http://www.tandfonline.com/loi/tcph20

Microfabricated ion traps

Marcus D. Hughes [a], Bjoern Lekitsch [a], Jiddu A. Broersma [a] & Winfried K. Hensinger [a]
[a] Department of Physics and Astronomy, University of Sussex, Brighton BN1 9QH, UK

Available online: 14 Sep 2011

To cite this article: Marcus D. Hughes, Bjoern Lekitsch, Jiddu A. Broersma & Winfried K. Hensinger (2011): Microfabricated ion traps, Contemporary Physics, 52:6, 505-529

To link to this article: http://dx.doi.org/10.1080/00107514.2011.601918

PLEASE SCROLL DOWN FOR ARTICLE

Full terms and conditions of use: http://www.tandfonline.com/page/terms-and-conditions

This article may be used for research, teaching, and private study purposes. Any substantial or systematic reproduction, redistribution, reselling, loan, sub-licensing, systematic supply, or distribution in any form to anyone is expressly forbidden.

The publisher does not give any warranty express or implied or make any representation that the contents will be complete or accurate or up to date. The accuracy of any instructions, formulae, and drug doses should be independently verified with primary sources. The publisher shall not be liable for any loss, actions, claims, proceedings, demand, or costs or damages whatsoever or howsoever caused arising directly or indirectly in connection with or arising out of the use of this material.

Contemporary Physics
Vol. 52, No. 6, November–December 2011, 505–529

Taylor & Francis
Taylor & Francis Group

Microfabricated ion traps

Marcus D. Hughes*, Bjoern Lekitsch, Jiddu A. Broersma and Winfried K. Hensinger

Department of Physics and Astronomy, University of Sussex, Brighton BN1 9QH, UK

(*Received 14 January 2011; final version received 20 June 2011*)

Ion traps offer the opportunity to study fundamental quantum systems with a high level of accuracy highly decoupled from the environment. Individual atomic ions can be controlled and manipulated with electric fields, cooled to the ground state of motion with laser cooling and coherently manipulated using optical and microwave radiation. Microfabricated ion traps hold the advantage of allowing for smaller trap dimensions and better scalability towards large ion trap arrays also making them a vital ingredient for next generation quantum technologies. Here we provide an introduction into the principles and operation of microfabricated ion traps. We show an overview of material and electrical considerations which are vital for the design of such trap structures. We provide guidance on how to choose the appropriate fabrication design, consider different methods for the fabrication of microfabricated ion traps and discuss previously realised structures. We also discuss the phenomenon of anomalous heating of ions within ion traps, which becomes an important factor in the miniaturisation of ion traps.

Keywords: ion traps; microfabrication; quantum information processing; anomalous heating; laser cooling and trapping

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

1. Introduction

Ion trapping was developed by Wolfgang Paul [1] and Hans Dehmelt [2] in the 1950s and 1960s and ion traps became an important tool to study important physical systems such as ion cavity QED [3,4], quantum simulators [5–9], determine frequency standards [10–13], as well as the development towards a quantum information processor [14–16]. In general, ion traps compare well to other physical systems with good isolation from the environment and long coherence times. Progress in many of the research areas where ion traps are being used may be aided by the availability of a new generation of ion traps with the ion–electrode distance on the order of tens of micrometres. While in some cases, the availability of micrometre scale ion–electrode distance and a particular electrode shape may be of sole importance, often the availability of versatile and scalable fabrication methods (such as micro-electromechanical systems (MEMS) and other micro-fabrication technologies) may be required in a particular field.

One example of a field which will see step-changing innovation due to the emergence of microfabricated ion traps is the general area of quantum technology with trapped ions. In 1995 David DiVincenzo set out criteria which determine how well a system can be used for quantum computing [17]. Most of these criteria have been demonstrated with an ion trap: qubit initialisation [18,19], a set of universal quantum gates creating entanglement between ions [14,20–22], long coherence times [23], detection of states [24,25] and a scalable architecture to host a large number of qubits [26–29]. An important research area is the development of a scalable architecture which can incorporate all of the DiVincenzo criteria. A realistic architecture has been proposed consisting of an ion trap array incorporating storage and gate regions [30–32] and could be implemented using microfabricated ion traps. Microfabricated ion traps hold the possibility of small trap dimensions on the order of tens of micrometres and more importantly fabrication methods like photolithography that allow the fabrication of very large scale arrays. Electrodes with precise shape, size and geometry can be created through a number of process steps when fabricating the trap.

In this article we will focus on the design and fabrication of microfabricated radio frequency (rf) ion traps as a promising tool for many applications in ion trapping. Another ion trap type is the Penning trap [33] and advances in their fabrication have been discussed by Castrejón-Pita et al. [34] and will not be discussed in this article. Radio-frequency ion traps include multi-layer designs where the ion is trapped between electrodes located in two or more planes with the

*Corresponding author. Email: m.d.hughes@sussex.ac.uk

ISSN 0010-7514 print/ISSN 1366-5812 online
© 2011 Taylor & Francis
http://dx.doi.org/10.1080/00107514.2011.601918
http://www.tandfonline.com

electrodes symmetrically surrounding the ion, for example as the ion trap reported by Stick et al. [26]. We will refer to such traps as symmetric ion traps. Geometries where all the electrodes lie in a single plane and the ion is trapped above that plane, for example as the trap fabricated by Seidelin et al. [27], will be referred to as asymmetric or surface traps.

There have been many articles discussing ion traps and related physics, including studies of fundamental physics [35–37], spectroscopy [38], and coherent control [15]. This article focuses on the current progress and techniques used for the realisation of microfabricated ion traps. First we discuss basic principles of ion traps and their operation in Section 2. Section 3 discusses linear ion trap geometries as a foundation of most ion trap arrays. The methodology of efficient simulation of electric fields within ion trap arrays is discussed in Section 4. Section 5 discusses some material characteristics that have to be considered when designing microfabricated ion traps including electric breakdown and rf dissipation. Section 6 provides a guide to realising such structures with the different processes outlined together with the capabilities and limitations of each one. Finally in Section 7 we discuss motional heating of the ion due to fluctuating voltage patches on surfaces and its implications for the design and fabrication of microfabricated ion traps.

2. Radio-frequency ion traps

Static electric fields alone cannot confine charged particles, this is a consequence of Earnshaw's theorem [39] which is analogous to Maxwell's equation $\nabla \cdot E = 0$. To overcome this Penning traps use a combination of static electric and magnetic fields to confine the ion [33,40]. Radio frequency (rf) Paul traps use a combination of static and oscillating electric fields to achieve confinement. We begin with an introduction into the operation of radio-frequency ion traps, highlighting important factors when considering the design of microfabricated ion traps.

2.1. Ion trap dynamics

First we consider a quadrupole potential within the radial directions, x- and y-axes, which is created from hyperbolic electrodes as shown in Figure 1, whilst there is no confinement within the axial (z) direction. By considering a static voltage V_0 applied to two opposite electrodes, the resultant electric potential will produce a saddle as depicted in Figure 2(a). With the ion present within this potential, the ion will feel an inward force in one direction and outward force in the direction perpendicular to the first. Reversing the

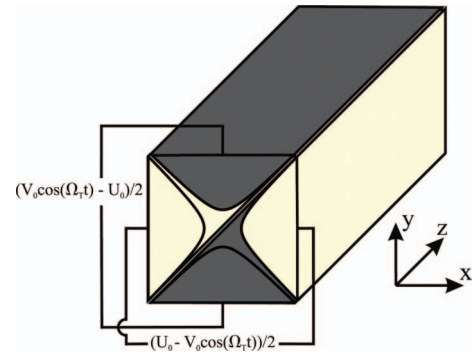


Figure 1. Hyperbolic electrodes where an rf voltage of V_0 cos (Ω_T t) together with a static voltage of U_0 is applied to two opposite electrodes. The polarity of this voltage is reversed and applied to the other set of electrodes.

polarity of the applied voltage the saddle potential will undergo an inversion as shown in Figure 2(b). As the force acting on the ion is proportional to the gradient of the potential, the magnitude of the force is less when the ion is closer to the centre. The initial inward force will move the ion towards the centre where the resultant outward force half a cycle later will be smaller. Over one oscillation the ion experiences a greater force towards the centre of the trap than outwards resulting in confinement. The effective potential the ion sees when in an oscillating electric field is shown in Figure 2(c). If the frequency of the oscillating voltage is too small then the ion will not be confined long enough in one direction. For the case where a high frequency is chosen then the effective difference between the inward and outward forces decreases and the resultant potential is minimal. By selecting the appropriate frequency Ω_T of this oscillating voltage together with the amplitude V_0 which is dependent on the mass of the charged particle, confinement of the particle can be achieved within the radial directions.

There are two ways to calculate the dynamics of an ion within a Paul trap, firstly a comprehensive treatment can be given using the Mathieu equation. The Mathieu equation provides a complete solution for the dynamics of the ion. It also allows for the determination of parameter regions of stability where the ion can be trapped. These regions of stability are determined by trap parameters such as voltage amplitude and rf drive frequency. Here we outline the process involved in solving the equation of motion via the Mathieu equation approach. By applying an oscillating potential together with a static potential, the total potential for the geometry in Figure 1 can be expressed as [36]

$$\phi(x, y, t) = (U_0 - V_0 \ \cos\ (\Omega_T t))\left(\frac{x^2 - y^2}{2r_0^2}\right), \qquad (1)$$

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

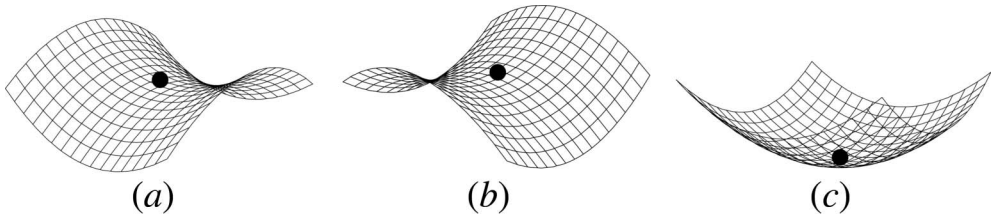


Figure 2. Principles of confinement with a pseudopotential. (*a*) A saddle potential created by a static electric field from a hyperbolic electrode geometry. (*b*) The saddle potential acquiring an inversion from a change in polarity. (*c*) The effective potential the ion sees resulting from the oscillating electric potential.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

where r_0 is defined as the ion–electrode distance. This is from the centre of the trap to the nearest electrode and Ω_T is the drive frequency of the applied time varying voltage. The equations of motion of the ion due to the above potential are then given by [36]

$$\frac{d^2x}{dt^2} = -\frac{e}{m}\frac{\partial\phi(x,y,t)}{\partial x} = -\frac{e}{mr_0^2}(U_0 - V_0 \cos \Omega_T t)x, \tag{2}$$

$$\frac{d^2y}{dt^2} = -\frac{e}{m}\frac{\partial\phi(x,y,t)}{\partial y} = \frac{e}{mr_0^2}(U_0 - V_0 \cos \Omega_T t)y, \tag{3}$$

$$\frac{d^2z}{dt^2} = 0. \tag{4}$$

Later it will be shown that the confinement in the z-axis will be produced from the addition of a static potential. Making the following substitution

$$a_x = -a_y = \frac{4eU_0}{mr_0^2\Omega_T^2}, \qquad q_x = -q_y = \frac{2eV_0}{mr_0^2\Omega_T^2},$$
$$\zeta = \Omega_T t/2,$$

Equations (2) and (3) can be written in the form of the Mathieu equation.

$$\frac{d^2i}{d\zeta^2} + (a_i - 2q_i \cos 2\zeta)i = 0, \qquad i = [x, y]. \tag{5}$$

The general Mathieu equation given by Equation (5) is periodic due to the $2q_i \cos 2\zeta$ term. The Floquet theorem [41] can be used as a method for obtaining a solution. Stability regions for certain values of the a and q parameters exist in which the ion motion is stable. By considering the overlap of both the stability regions for the x- and y-axes of the trap [36,37], the parameter region where stable trapping can be accomplished is obtained. For the case when $a = 0$, $q \ll 1$ then the motion of the ion in the x-axis can be described as follows,

$$x(t) = x_0 \cos(\omega_x t)\left[1 + \frac{q_x}{2}\cos(\Omega_T t)\right] \tag{6}$$

with the equation of motion in the y-axis of the same form. The motion of the ion is composed of secular motion ω_x (high amplitude slow frequency) and micromotion at the drive frequency Ω_T (small amplitude high frequency).

The second form to calculate motion is the pseudopotential approximation [2]. This considers the time averaged force experienced by the ion in an inhomogeneous field. With an rf voltage of $V_0 \cos \Omega_T t$ applied to the trap a solution for the pseudopotential approximation is given by [2]

$$\psi(x,y,z) = \frac{e^2}{4m\Omega_T^2}|\nabla V(x,y,z)|^2, \tag{7}$$

where m is the mass of the ion, $\nabla V(x,y,z)$ is the gradient of the potential. The motion of the ion in a rf potential can be described just by the secular motion in the limit where $q_i/2 \equiv 2^{1/2}\omega_i/\Omega_T \ll 1$. The secular frequency of the ion is given by [42]

$$\omega_i^2(x,y,z) = \frac{e^2}{4m^2\Omega_T^2}\frac{\partial^2}{\partial x^2}(|\nabla V(x,y,z)|^2). \tag{8}$$

The pseudopotential approximation provides a means to treat the rf potential in terms of electrostatics only, leading to simpler analysis of electrode geometries.

Micromotion can be divided into intrinsic and extrinsic micromotion. Intrinsic micromotion refers to the driven motion of the ion when displaced from the rf nil position due to the secular oscillation within the trap. Extrinsic micromotion describes an offset of the ion's position from the rf nil from stray electric fields, this can be due to imperfections of the symmetry in the construction of the trap electrodes or the build up of charge on dielectric surfaces. Micromotion can cause a problem with the widening of atomic transition linewidth, second-order Doppler shifts and reduced lifetimes without cooling [43]. It is therefore important when designing ion traps that compensation of stray electric fields can occur in all directions of motion. Another important factor is the occurrence of a possible phase difference φ between the rf voltages

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

on different rf electrodes within the ion trap. This will result in micromotion that cannot be compensated for. A phase difference of $\varphi = 1^\circ$ can lead to an increase in the equivalent temperature for the kinetic energy due to the excess micromotion of 0.41 K [43], well above the Doppler limit of a few milli-kelvin.

The trap depth of an ion trap is the potential difference between pseudopotential at the minimum of the ion trap and the lowest turning point of the potential well. For hyperbolic geometries this is at the surface of the electrodes, for linear geometries (see Section 3.1) it can be obtained through electric field simulations. Higher trap depths are preferable as they allow the ion to remain trapped longer without cooling. Typical trap depths are on the order of a few eV. The speed of optical qubit gates for quantum information processing [44] and shuttling within arrays [45] is dependent on the secular frequency of the ion trap. Secular frequencies and trap depth are a function of applied voltage, drive frequency Ω_T, the mass of the ion m and the particular geometry (particularly the ion–electrode distance). Since the variation of the drive frequency is limited by the stability parameters, it is important to achieve large maximal rf voltages for the design of microfabricated ion traps, which is typically limited by bulk breakdown and surface flashover (see Section 5). It is also important to note that the secular frequency also increases whilst scaling down trap dimensions for a given applied voltage allowing for large secular frequencies at relatively small applied voltages.

2.2. *Motional and internal states of the ion.*

Single ions can be considered to be trapped within a three-dimensional harmonic well with the three directions of motion uncoupled. Considering the motion of the ion along one of the axes, the Hamiltonian describing this model can be represented as

$$H = \hbar\omega\left(a^\dagger a + \frac{1}{2}\right) \tag{9}$$

with ω the secular frequency, $a^\dagger$ and a the raising and lowering operators, respectively; these operators have the following properties: $a^\dagger|n\rangle = (n+1)^{1/2}|n+1\rangle$, $a|n\rangle = n^{1/2}|n-1\rangle$. When an ion moves up one motional level, it is said to have gained one motional quantum of kinetic energy. For most quantum gates with trapped ions, the ion must reside within the Lambe–Dicke regime. This is where the ion's wave function spread is much less than the optical wavelength of the photons interacting with the ion. The original proposed gates [30] required the ion to be in the ground state motional energy level, but more robust schemes [21] do not have such stringent requirements anymore.

Another requirement for many quantum technology application is the availability of a two-level system for the qubit to be represented, such that the ion's internal states can be used for encoding. The qubit can then be initialised into the state $|1\rangle$, $|0\rangle$ or a superposition of both. Typical ion species used are hydrogenic ions, which are left with one orbiting electron in the outer shell and similar structure to hydrogen once ionised. These have the simplest lower level energy diagrams. Candidates for ions to be used as qubits can be subdivided into two categories. Hyperfine qubits, $^{171}Yb^+$, $^{43}Ca^+$, $^{9}Be^+$, $^{111}Cd^+$, $^{25}Mg^+$ use the hyperfine levels of the ground state and have lifetimes on the order of thousands of years, whilst optical qubits, $^{40}Ca^+$, $^{88}Sr^+$, $^{172}Yb^+$ use a ground state and a metastable state as the two-level system. These metastable states typically have lifetimes on the order of seconds and are connected via optical transitions to the other qubit state.

2.3. *Laser cooling*

For most applications, the ion has to be cooled to a state of sufficiently low motional quanta, which can be achieved via laser cooling. For a two-level system, when a laser field with a frequency equivalent to the spacing between the two energy levels is applied to the ion, photons will be absorbed resulting in a momentum 'kick' onto the ion. The photon is then spontaneously emitted which leads to another momentum kick onto the ion in a completely random direction so the net effect of many photon emissions averages to zero. Due to the motion of the ion within the harmonic potential the laser frequency will undergo a Doppler shift. By red detuning (lower frequency) the laser frequency by δ from resonance, Doppler cooling can be achieved. When the ion moves towards the laser, the ion will experience a Doppler shift towards the resonant transition frequency and more scattering events will occur with the net momentum transfer slowing the ion down. Less scattering events will occur when travelling away from the Doppler shifted laser creating a net cooling of the ion's motion. Doppler cooling can typically only achieve an average motional energy state $\bar{n} > 1$. In order to cool to the ground state of motion, resolved sideband cooling can be utilised. This can be achieved with stimulated Raman transitions [46,47].

For effective cooling of the ion, the **k**-vector of the laser needs a component in all three directions of uncoupled motion. These directions depend on the trap potential and they are called the principal axes. For a convenient choice of directions for the laser beam, principal axes can be rotated by an angle θ by application of appropriate voltages [42,48] or asymmetries in the geometry about the ion's position [49–51].

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

The angle of rotation of the principal axes can be obtained through the Hessian matrix of the electric field. This angle describes a linear transformation of the electric potential that eliminates any cross-terms between the axes creating uncoupled equations of motion. The eigenvectors of the matrix signify the direction of the principal axes.

2.4. *Operation of microfabricated ion traps*

In order to successfully operate a microfabricated ion trap a certain experimental infrastructure needs to be in place, from the ultra high vacuum (UHV) system apparatus to the radio-frequency source. A description of experimental considerations for the operation of microfabricated ion traps was given by McLoughlin et al. [52]. For long storage times of trapped ions and performing gate operations, the collision with background particles must not be a limiting factor. Ion traps are therefore typically operated under ultra high vacuum (UHV) (pressures of $10^{-9}-10^{-12}$ mbar). The materials used need to be chosen carefully such that outgassing does not pose a problem. The materials used for different trap designs are discussed in more detail within Section 6.

To generate the high rf voltage ($\sim$100–1000 V) a resonator [53] is commonly used. Typical resonator designs include helical and coaxial resonators. The advantage of using a resonator, is that it provides a frequency source with a narrow bandpass, defined by the quality factor Q of the combined resonator–ion trap circuit. This provides a means of filtering out frequencies that couple to the motion of the ion leading to motional heating of the trapped ion. A resonator also fulfills the function of impedance matching the frequency source to the ion trap. The total resistance and capacitance of the trap lowers the Q factor. It is important to minimise the resistance and capacitance of the ion trap array if a high Q value is desired.

To provide electrical connections, ion traps are typically mounted on a chip carrier with electrical connections provided by wire bonding individual electrodes to an associate connection on the chip carrier. Bond pads on the chip are used to provide a surface on which the wire can be connected, see Figure 3. The pins of the chip carrier are connected to wires which pass to external voltage supplies outside the vacuum system.

The loading of atomic ions within Paul traps is performed utilising a beam of neutral atoms typically originating from an atomic oven consisting of a resistively heated metallic tube filled with the appropriate atomic species or its oxide. The atomic flux is directed to the trapping region where atoms can be ionised via electron bombardment or more commonly by photoionisation, see for example [52,54]. The latter has the advantage of faster loading rates requiring lower neutral atom pressures and results in less charge build up resulting from electron bombardment. For asymmetric traps in which all the electrodes lie in the same plane, see Figure 4, a hole within the electrode structure can be used for the atomic flux to pass through the trap structure, this is defined as backside loading [49]. The motivation behind this method is to reduce the coating of the electrodes and more importantly reduce coating of the notches between the electrodes from the atomic beam reducing charge build up and the possibility of shorting between electrodes. However, the atomic flux can also be directed parallel to the surface in an asymmetric ion trap due to the low atomic flux required for photoionisation loading.

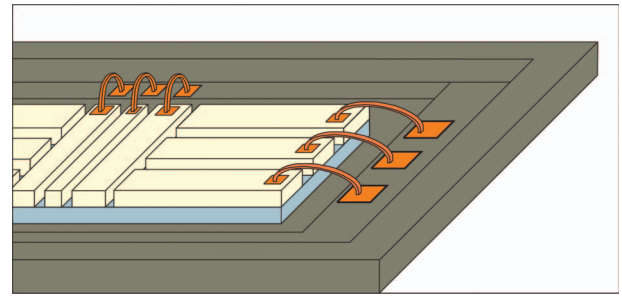


Figure 3. Wire bonding a microfabrciated chip to a chip carrier providing external electrical connections.

3. Linear ion traps

The previously mentioned ideal linear hyperbolic trap only provides confinement within the radial directions and does not allow for optical access. By modifying the geometry as depicted in Figure 4 linear ion traps are created. To create an effective static potential for the confinement in the axial (z-axis) direction, the associate electrodes are segmented. This allows for the creation of a saddle potential and when superimposed onto rf pseudopotential provides trapping in three dimensions. By selecting the appropriate amplitudes for the rf and static potentials such that the radial secular frequencies ω_x, ω_y are significantly larger than the axial frequency ω_z, multiple ions will form a linear chain along the z-axis. The motion of the ion near the centre of the trap can be considered to be harmonic as a very good approximation. The radial secular frequency of a linear trap is on the order of that of a hyperbolic ion trap of same ion–electrode distance but different by a geometric factor η [42].

3.1. *Linear ion trap geometries*

Linear ion trap geometries can be realised in a symmetric or asymmetric design as depicted in Figure 4.

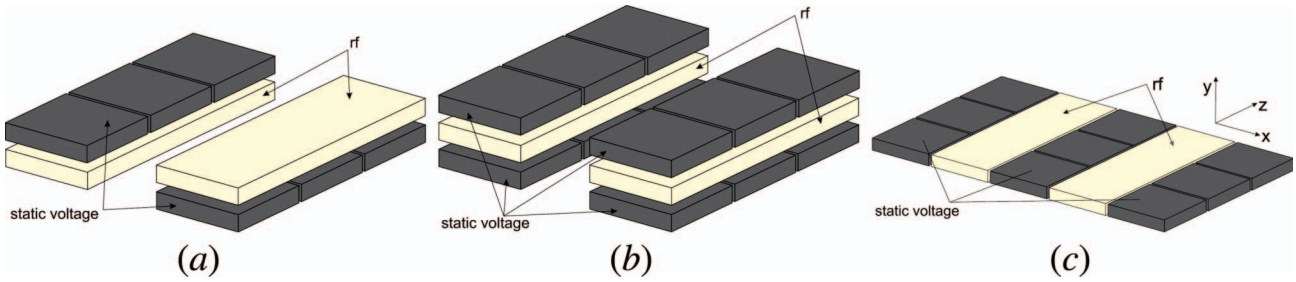


Figure 4. Different linear trap geometries. (*a*) A two-layer design in which the rf electrodes (yellow) are diagonally opposite and the dc electrodes (grey) are segmented. (*b*) A three-layer design in which the rf electrodes are surrounded by the dc electrodes. (*c*) A five-wire asymmetric design where all the electrodes lie in the same plane.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

In symmetric designs the ions are trapped between the electrodes, as shown for two- and three-layer designs in Figure 4(*a*) and (*b*), respectively. These types of designs offer higher trap depths and secular frequencies compared to asymmetric traps of the same trap parameters. Two-layer designs offer the highest secular frequencies and trap depths whilst three-layer designs offer more control of the ions position for micromotion compensation and shuttling.

The aspect ratio for symmetric designs is defined as the ratio of the separation between the two sets of electrodes w and the separation of the layers d depicted in Figure 5. As the aspect ratio rises, the geometric efficiency factor η decreases and approaches asymptotically $1/\pi$ for two-layer designs [42]. Another advantage of symmetric traps is more freedom of optical laser access, allowing laser beams to enter the trapping zone in various angles. In asymmetric trap structures the laser beams typically have to enter the trapping zone parallel to the trap surface. Asymmetric designs offer the possibility of simpler fabrication processes. Buried wires [50] and vertical interconnects can provide electrical connections to electrodes which cannot be connected via surface pathways. Trap depths are typically smaller than for symmetric ion traps, therefore higher voltages need to be applied to obtain the same trap depth and secular frequencies of an equivalent symmetric ion trap. The widths of the individual electrodes can be optimised to maximise trap depth [51].

In order to successfully cool ions, Doppler cooling needs to occur along all three principal axes therefore the $\boldsymbol{k}$-vector of the laser needs to have a component along all the principal axes. Due to the limitation of the laser running parallel to the surface it is important that all principal axes have a component along the $\boldsymbol{k}$-vector of the Doppler cooling laser beam. Five-wire designs (Figure 6(*b*) and (*c*)) have a static voltage electrode below the ion position, surrounded by rf electrodes and additional static voltage electrodes. With the rf electrodes of equal width (Figure 6(*b*)) one

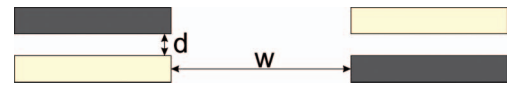


Figure 5. For two-layer traps the aspect ratio is defined as w/d.

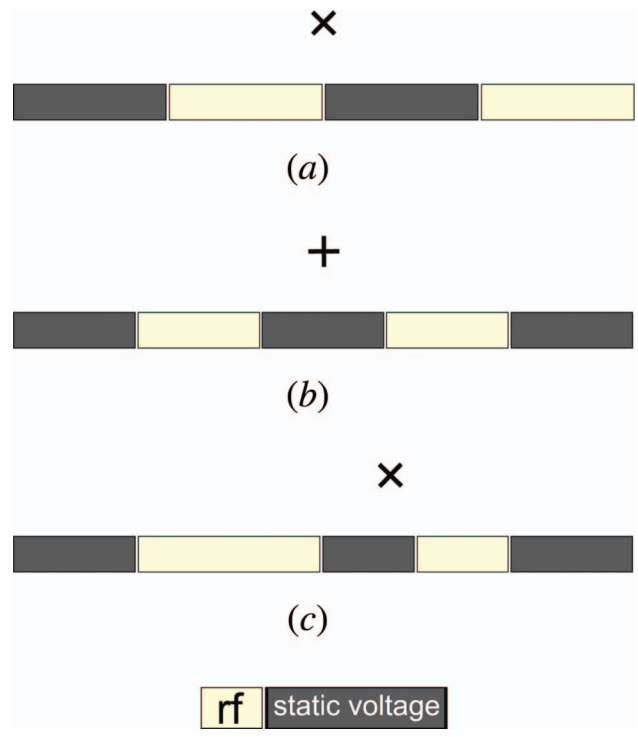


Figure 6. Cross-section in the $x-y$ plane of the different types of asymmetric designs. (*a*) Four-wire design in which the principal axes are naturally non-perpendicular with respect to the plane of the electrodes. (*b*) Five-wire design where the electrodes are symmetric and one principal axis is perpendicular to the surface. (*c*) Five-wire design with different widths rf electrodes, this allows the principal axes to be rotated.

of the principal axes is perpendicular to the surface of the trap. However, it can be rotated via utilising two rf electrodes of different width (Figure 6(*c*)) or via

splitting the central electrodes [48]. A four-wire design shown in Figure 6(*a*) has the principal axes naturally rotated but the ion is in direct sight of the dielectric layer below since the ion is located exactly above the trench separating two electrodes. Deep trenches have been implemented [49,55] to reduce the effect of exposed dielectrics.

3.2. *From linear ion traps to arrays*

For ions stored in microfabricated ion traps to become viable for quantum information processing, thousands or even millions of ions need to be stored and interact with each other. This likely requires a number of individual trapping regions that is on the same order as the number of ions and furthermore, the ability for the ions to interact with each other so that quantum information can be exchanged. This could be achieved via arrays of trapping zones that are connected via junctions. To scale up to such an array requires fabrication methods that are capable of producing large scale arrays without requiring an unreasonable overhead in fabrication difficulty. This makes some fabrication methods more viable for scalability than other techniques. An overview of different fabrication methods is discussed in more detail within Section 6.

The transport of ions through junctions was first demonstrated within a three-layer symmetric design [28] and later near-adiabatic in a two-layer symmetric trap array [29], shown in Figure 7(*a*) and (*b*). Both ion trap arrays were made from laser machined alumina substrates incorporating mechanical alignment. The necessity of mechanical alignment and laser machining limit the opportunity to scale up to much larger numbers of electrodes making other microfabrication methods more suitable in the long term. Transport through an asymmetric ion trap junction (Figure 7(*c*)) was then demonstrated by Amini et al. [50], however, this non-adiabatic transport required continuous laser cooling. Wesenberg carried out a theoretical study [56] of how one can implement optimal ion trap array intersections. Splatt et al. demonstrated reordering of ions within a linear trap [57].

4. Simulating the electric potentials of ion trap arrays

Accurate simulations of the electric potentials are important for determining trap depths, secular frequencies and to simulate adiabatic transport including the separation of multiple ions and shuttling through corners [45,58]. Various methods can be used in determining the electric potentials from the trap electrodes, with both analytical and numerical methods available. Numerical simulations using the finite element method (FEM) and the boundary element method (BEM) [45,59] provide means to obtain the full 3D potential of the trap array. FEM works by dividing the region of interest into a mesh of nodes and vertices, an iterative process then finds a solution which connects the nodes whilst satisfying the boundary conditions and a potential can be found for each node. BEM starts with the integral equation formulation of Laplace's equation resulting in only surface integrals being non-zero in an empty ion trap. Due to BEM solving surface integrals, this is a dimensional order less than FEM thus providing a more efficient numerical solution than FEM [45]. To obtain the total potential the basis function method is used [45]. A basis function for a particular electrode is obtained by applying 1 V to one particular electrode whilst holding the other electrodes at ground. By summing all the basis functions (with each basis function multiplied by the actual voltage for the particular electrode) the total trapping potential can be obtained.

For the case of asymmetric ion traps, analytical methods provide means to calculate the trapping potential significantly faster allowing for optimisation of the electrode structures. A Biot-Savart-like law [60] can be used and is related to the Biot-Savart law for

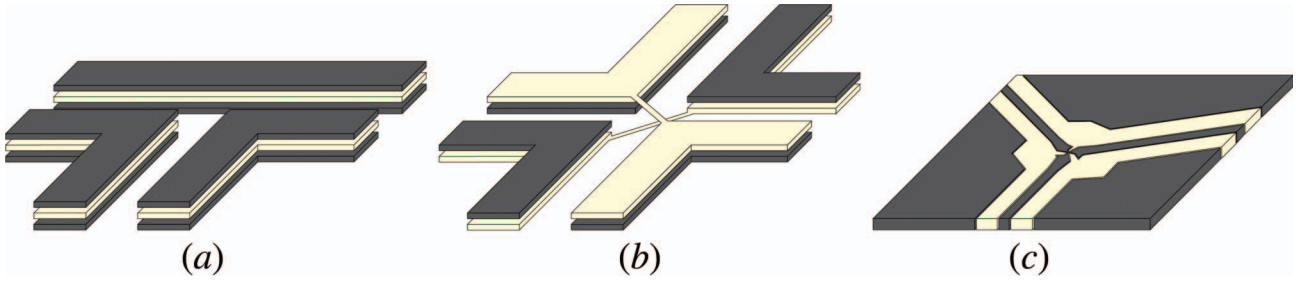


Figure 7. Junctions that have been used to successfully shuttle ions. The yellow parts represent the rf electrodes. No segmentation of the static voltage electrodes (grey) is shown. (*a*) T-junction design [28] where corner shuttling and swapping of two ions were demonstrated for the first time. While the transport was reliable the ion gained a significant amount of kinetic energy during a corner-turning operation. (*b*) A two-layer X-junction [29] was used to demonstrate highly reliable transport through a junction with a kinetic energy gain of only a few motional quanta. (*c*) A Y-junction [50] was used to demonstrate transport through an asymmetric junction design, however, requiring continuous laser cooling during the shuttling process.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

magnetic fields in which the magnetic field at a point of interest is obtained by solving the line integral of an electrical current around a closed loop. This analogy is then applied to electric fields in the case of asymmetric ion traps [61]. One limitation for these analytical methods is the fact that all the electrodes must lie in a single plane, with no gaps, which is referred to as the gapless plane approximation. House [62] has obtained analytical solutions to the electrostatic potential of asymmetric ion trap geometries with the electrodes located on a single plane within a gapless plane approximation. Microfabrication typically requires gaps of a few micrometres [49] which need to be created to allow for different voltages on neighbouring electrodes. The approximation is suggested to be reasonable for gaps much smaller than the electrode widths and studies into the effect of gapped and finite electrodes have been conducted [63]. However, within the junction region where electrodes can be very small and high accuracy is required, the gapless plane approximation may not necessarily be sufficient.

5. Electrical characteristics

5.1. *Voltage breakdown and surface flashover*

Miniaturisation of ion traps is not only limited by the increasing motional heating of the ion (see Section 7), but also by the maximum applied voltages allowed by the dielectrics and gaps separating the electrodes. Both secular frequency and trap depth depend on the applied voltage. Therefore, it is important to highlight important aspects involved in electrical breakdown. Breakdown can occur either through the bulk material, a vacuum gap between electrodes, or across an insulator surface (surface flashover). There are many factors which contribute to the breakdown of a trap, from the specific dielectric material used and its deposition process, residues on insulating materials to the geometry of the electrodes itself and the frequency of the applied voltage.

Bulk breakdown describes the process of breakdown via the dielectric layer between two independent electrodes. An important variable which has been modelled and measured is the dielectric strength. This is the maximum field that can be applied before breakdown occurs. The breakdown voltage V_c is related to the dielectric strength for an ideal capacitor by $V_c = dE_c$, where d is the thickness of the dielectric. There have been many studies into dielectric strengths showing an inverse power law relation $E_c \propto d^{-n}$ [64–70]. The results show a typical range of values (0.5 – 1) for the scaling parameter n. Although decreasing the thickness will increase the dielectric strength this will not increase the breakdown voltage if the scaling parameter lies below one.

Surface flashover occurs over the surface of the dielectric material between two adjacent electrodes. The topic has been reviewed [71] with studies showing a similar trend with a distance dependency on the breakdown voltage with $V_b \propto d^{\alpha}$ where $\alpha \approx 0.5$ [70,72]. Surface flashover usually starts from electron emission from the interface of the electrode, dielectric and vacuum known as the triple point. Imperfections at this point increase the electric field locally and will reduce the breakdown voltage. The electric field strength for surface breakdown has been measured to be a factor of 2.5 less than that for bulk breakdown of the same material, dimensions and deposition process [70], with thicknesses of 1–3.9 μm for substrate breakdown and lengths of 5–600 μm considered.

The range of parameters that can affect breakdown from the difference between rf and applied static voltages [26,72,73] includes the dielectric material, deposition process and the geometry of the electrodes [71]. Therefore, it is most advisable to carry out experimental tests on a particular ion trap fabrication design to determine reliable breakdown parameters. In a particular design it is very important to avoid sharp corners or similar features as they will give rise to large local electric fields at a given applied voltage.

5.2. *Power dissipation and loss tangent*

When scaling to large trap arrays the finite resistance R and capacitance C of the electrodes as well as the dielectric materials within the trap structure result in losses and therefore have to be taken into account when designing an ion trap. The power dissipation, which results from rf losses, is highly dependent on the materials used and the dimensions of the trap structure and can result in heating and destruction of trap structures. To calculate the power dissipated in a trap a simple lumped circuit model, as shown in Figure 8, can be utilised.

The dielectric material insulating the electrodes cannot be considered a perfect insulator resulting in a complex permittivity ε, with $\varepsilon = \varepsilon' + i\varepsilon''$. Lossless parts are represented by ε' and lossy parts by ε''. Substituting this into Ampère's circuital law and by rearranging one obtains [74]

$$\nabla \times H = [(\sigma + \omega\epsilon'') - i\omega\epsilon']E. \tag{10}$$

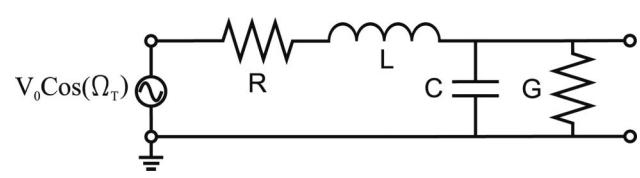


Figure 8. The rf electrode modelled with resistance R, capacitance C, inductance L and conductance G.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

σ is the conductivity of the dielectric for an applied alternating current, and ω is the angular frequency of the applied field. The effective conductance is often referred to as $\sigma' = \sigma + \omega\varepsilon''$. The ratio of the conduction to displacement current densities is commonly defined as loss tangent tan δ

$$\tan\,\delta = \frac{\sigma + \omega\epsilon''}{\omega\epsilon'}. \tag{11}$$

For a good dielectric the conductivity σ is much smaller then $\omega\varepsilon''$ and we can then make the following approximation $\tan\delta = \varepsilon''/\varepsilon'$. For a parallel plate capacitor the real and imaginary parts of the permittivity can be expressed as [75]

$$\varepsilon' = \frac{Cd}{\varepsilon_0 A}, \qquad \varepsilon'' = \frac{Gd}{\varepsilon_0 \omega A}. \tag{12}$$

Substituting this into the approximated loss tangent expression, the conductance G can be expressed as

$$G = \omega C\,\tan\,\delta. \tag{13}$$

Now we can calculate the power dissipated through the rf electrodes driven by frequency $\omega = \Omega_T$, with $I_{\rm rms} = V_{\rm rms}/Z$. The total impedance for this circuit is

$$Z = R - \mathrm{i}\omega L + \frac{G + \mathrm{i}\omega C}{G^2 + \omega^2 C^2}. \tag{14}$$

The second term of the impedance represents the inductance L of the electrodes, which we approximate with the inductance of two parallel plates separated by a dielectric with $L = \mu l(d/w)$ [76]. Assuming a dielectric of thickness $d \approx 10\ \mu$m, electrode width $w \approx 100\ \mu$m, electrode length $l \approx 1$ mm, magnetic permeability of the dielectric $\mu \approx 10^{-6}(H/m)$ [77], the inductance can be approximated to be $L \approx 10^{-10}$ H. Comparing the imaginary impedance terms $\mathrm{i}\omega L$ and $\mathrm{i}\omega[C/(G^2 + \omega^2 C^2)]$, it becomes clear that the inductance can be neglected. The average power dissipated in a lumped circuit is given by $P_{\rm d} = \mathrm{Re}(V_{\rm rms} I^*_{\rm rms})$ [78]. Using the approximation for the total impedance $Z = R + [(G + \mathrm{i}\omega c)/(G^2 + \omega^2 C^2)]$ we obtain

$$P_d = \frac{V_0^2 R(G^2 + C^2\omega^2)^2}{2(C^2\omega^2 + R^2(G^2 + C^2\omega^2)^2)} \tag{15}$$

and using Equation (13) one obtains

$$P_d = \frac{V_0^2 \Omega_T^2 C^2 R(1 + \tan^2\delta)^2}{2(1 + \Omega_T^2 C^2 R^2 (1 + \tan^2\delta)^2)}. \tag{16}$$

In the limit where $\tan\delta$ and $\Omega_T CR \ll 1$, the dissipated power can be simplified as $P_d = \frac{1}{2} V_0^2 \Omega_T^2 C^2 R$. Considering Equation (16), important factors to reduce power dissipation are an electrode material with low resistivity, a low capacitance of the electrode geometry and a dielectric material with low loss tangent at typical drive frequencies ($\Omega_T = 10$–80 MHz).

Values for loss tangent have been studied in the GHz range for microwave integrated circuit applications [79] and diode structures at kHz range [75,80,81]. Generally the loss tangent decreases with increasing frequency [82,83] and there has been a temperature dependence shown for specific structures [80]. Values at 1 MHz can be obtained but are dependent on the structures tested; Au/SiO_2/n-Si $\tan\delta \sim 0.05$ [75], Au/Si_3N_4/p-Si $\tan\delta \sim 0.025$ [81], Cr/$SiO_{1.4}$/Au $\tan\delta \sim 0.09$ [84]. The loss tangent will be dependent on the specific structure and also dependent on the doping levels. It is suggested that the loss tangent for specific materials be requested from the manufacturer or measured for the appropriate drive frequency. For optimal trap operation, careful design considerations have to be made to reduce the overall resistance and capacitance of the trap structure minimising the dissipated power.

6. Fabrication processes

Using the information given in the previous sections about ion trap geometries, materials and electrical characteristics, common microfabrication processes can be discussed. One of the main criteria for choice of fabrication process is the compatibility with a desired electrode geometry. Asymmetric and symmetric geometries result in different requirements and therefore we will discuss them separately. First, process designs for asymmetric traps will be discussed followed by symmetric ion trap designs and universally compatible processes. The compatibility of a process with discussed materials, and geometries will be highlighted. Structural characteristics and limitations of a process will be explained and solutions will then be given. As the exact fabrication steps depend on materials used and available equipment, the process sequences will be discussed as generally possible. However, to give the reader a guideline of possible choices, material and process step details of published ion traps will be given in brackets. The discussion will start with a simple process that can be performed in a wide variety of laboratories and is offered by many commercial suppliers.

6.1. Printed circuit board (PCB)

The first discussed fabrication technique used for ion trap microfabrication is the widely available Printed Circuit Boards (PCB) process. This technology is commonly used to create electrical circuits for a wide variety of devices and does not require cleanroom

technology. For ion traps generally a monolithic single or two layer PCB process is used. Monolithic processes rely on the fabrication of ion trap structures by adding to or subtracting material from one component. In contrast to this, wafer bonding, mechanical mounting or other assembly techniques are used to fabricate traps from pre-structured, potentially monolithic parts in a non-monolithic process. When combined with cleanroom fabrication such a process can be used for very precise and large scale structures, however, mechanical alignment remains an issue.

PCB processes commonly allow for minimal structure sizes of approximately 100 μm [85] and slots milled into the substrate of 500 μm width. This limits the uses of this technique for large and complex designs but also results in a less complex and easier accessible process. Smaller features are possible with special equipment, which is not widely available. The following section will give a general introduction into the PCB processes used to manufacture ion traps.

This process is based on removing material instead of depositing materials as used in most cleanroom processes. Therefore, the actual process sequence starts by selecting a suitable metal coated PCB substrate. The substrate has to exhibit the characteristics needed for ion trapping, ultra high vacuum (UHV) compatibility, low rf loss tangent and high breakdown voltage (commercially available high-frequency (hf) Rogers 4350B used in [85]). One side of the PCB substrate is generally pre-coated with a copper layer by the manufacturer, which is partially removed in the process to form the trap structures as shown in Figure 9(*c*). Possible techniques to do this are mechanical milling shown in Figure 9(*b*) or chemically wet etching using a patterned mask. The mask can either be printed directly onto the copper layer or photolithography can be used to pattern photo resist as shown in Figure 9(*a*). To reduce exposed dielectrics and prevent shorting from material deposited in the trapping process, slots can be milled into the substrate underneath the trapping zones as shown in Figure 9(*d*).

The fabricated electrodes form one plane and make the process unusable for symmetric ion traps (SIT). Not only are the electrodes located in one plane they also sit directly on the substrate, which makes a low rf loss tangent substrate necessary to minimise energy dissipation from the rf rails into the substrate. As explained in Section 5.2 high power dissipation leads to an increase of the temperature of the ion trap structure and also reduces the quality factor of the loaded resonator. PCB substrates intended for hf devices generally exhibit a low rf loss tangent (values of $\tan\delta = 0.0031$ are typical [87]) and many are UHV compatible, therefore can be used for ion traps. Other factors reducing the quality factor are the resistances and capacitances of the electrodes. When slots are milled into the substrate exposed dielectrics underneath the ion can be avoided despite the electrode structures being formed directly on the substrate. The otherwise exposed dielectrics would lead to charge built up underneath the ion resulting in stray fields pushing the ion out of the rf nil and leading to micromotion. By relying on widely available fabrication equipment this technique enabled the realisation of several ion trap designs with micrometre-scale structures, published in [57,85,86,88,89], without the need for cleanroom techniques.

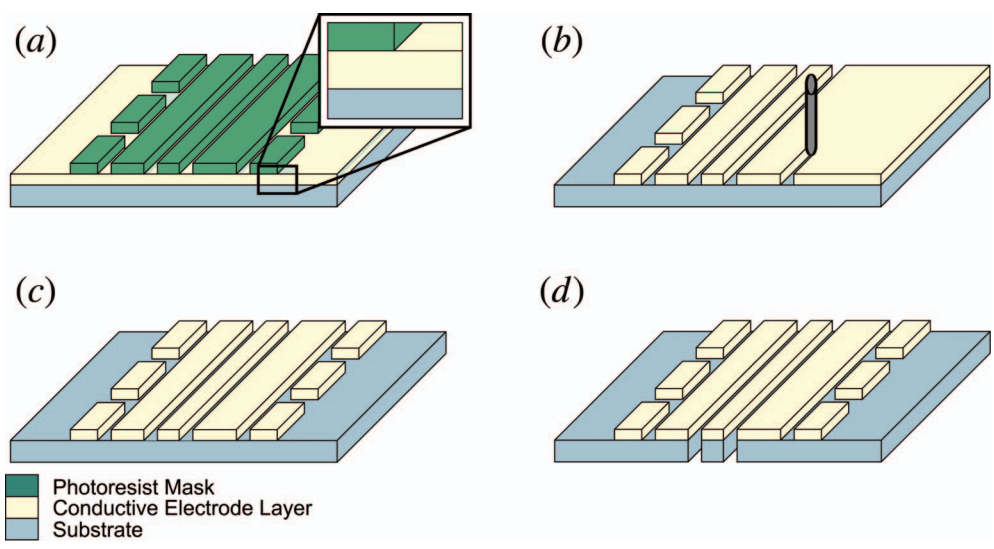


Figure 9. Overview of several PCB fabrication processes. (*a*) Deposition and exposure of the resist used as a mask in later etch steps. (*b*) Removal of the top copper layer using mechanical milling. (*c*) Removal of the copper layer using a chemical wet etch and later removal of the deposited mask. (*d*) Mechanical removal of the substrate underneath the trapping zone [86].

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

The discussed single layer PCB process can be used for electrode geometries including y-junctions and linear sections. More complex topologies with isolated electrodes and buried wires require a more complex two-layer process. To address limitations caused by the minimal structure separations and sizes allowing for ion traps with higher electrode and trapping-zone densities, a process based on common cleanroom technology will be discussed next.

6.2. *Conductive structures on substrate (CSS)*

Common cleanroom fabrication techniques like high resolution photolithography, isotropic and anisotropic etching, deposition, electroplating and epitaxial growth allow a very precise fabrication of large scale structures. The monolithic technique we discuss here is based on a 'conductive structures on substrate' process and was used to fabricate the first microfabricated asymmetric ion trap (AIT) [27]. Electrode structures separated by only 5 μm [48] can be achieved with this process and smaller structures are not limited by the process but flashover and bulk breakdown voltage of the used materials. The structures are formed by means of deposition and electroplating of conductive material onto a substrate instead of removing precoated material. This makes it possible to use a much wider variety of materials in a low number of process steps. Several variations or additions were published [27,90–93] to adjust the process for optimal results with desired materials and structures.

First the standard process will be presented, which starts by coating the entire substrate (for example, polished fused quartz as used in [27]) with a metal layer working as a seed layer (0.1 μm copper), necessary for a following electroplating step. Commonly an adhesion layer (0.03 μm titanium) is evaporated first, as most seed layer materials ([27,92]) have a low adhesion on common substrates, see Figure 10(*a*). Then a patterned mask (photolithographic structured photo resist) with a negative of the electrode structures is formed on the seed layer. The structures are then formed by electroplating (6 μm gold) metal onto the seed layer, see Figure 10(*b*). Afterwards the patterned mask is no longer needed and removed. The seed layer, providing electrical contact between the structures during electroplating, also needs to be removed to allow trapping operations. This can be done using the electroplated electrodes as a mask and an isotropic chemical wet etch process to remove the material, see Figure 10(*c*). Then the adhesion layer is removed in a similar etch process (for example using hydrofluoric acid) and the completed trapping structure is shown in Figure 10(*d*).

Depending on the available equipment additional or different steps can be performed, which also allow special features to be included on the chip. One variation was published in [92] replacing the seed layer with a thicker metal layer (1 μm silver used in [92]) and forming the patterned mask on top of that, as shown in Figure 11(*a*). The electrode structures are then formed by using this mask to wet etch through the thick silver layer (NH3OH: H2O2 silver etch) and the adhesion layer (hydrofluoric acid) Figure 11(*b*). To counter potentially sharp electrode edges resulting from the wet etch process an annealing step (720°C to 760°C for 1 h)

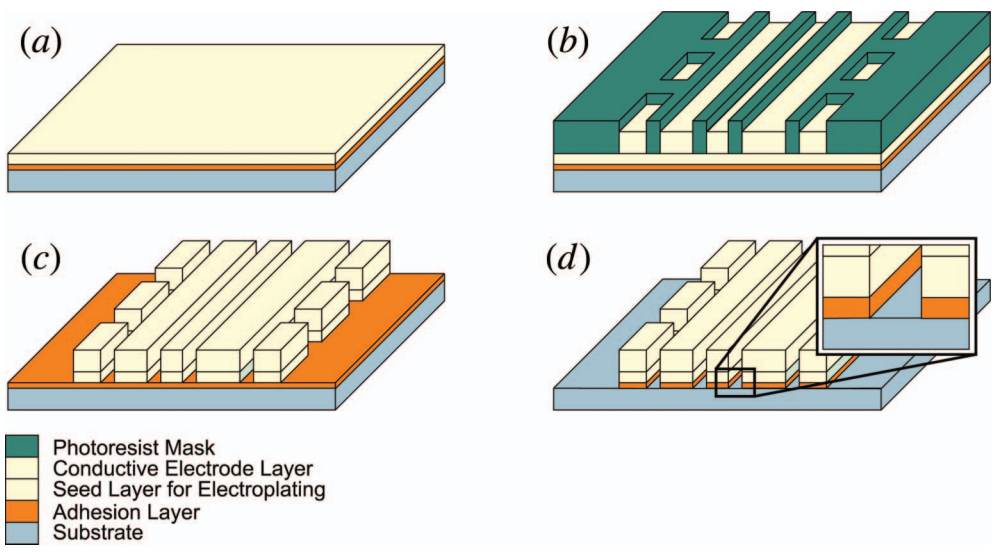


Figure 10. Fabrication sequence of the standard 'Conductive Structures on Substrate' process. (*a*) The sequence starts with the deposition of an adhesion and seed layer. (*b*) An electroplating step creating the electrodes using a patterned mask. (*c*) Removal of the mask followed by a first etch step removing the seed layer. (*d*) Second etch step removing the adhesion layer.

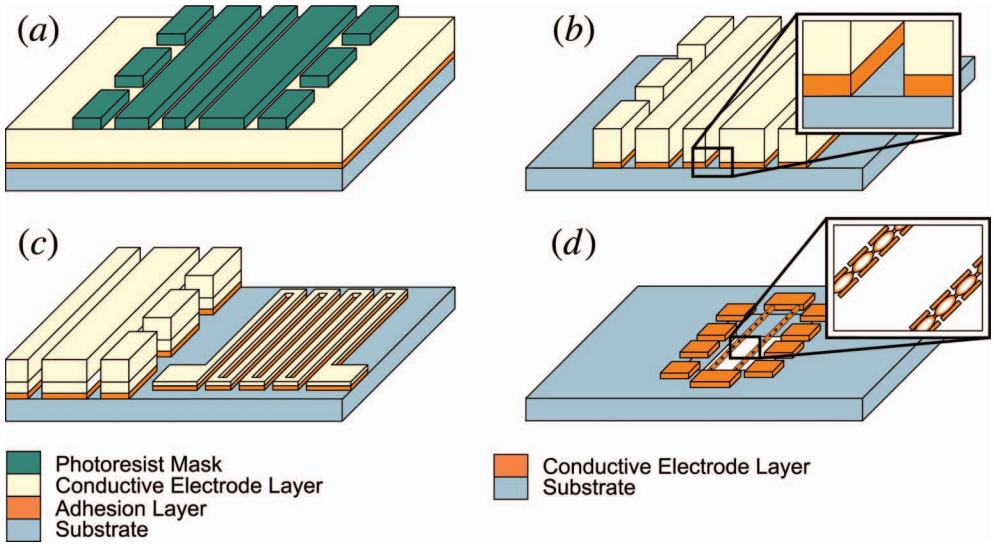


Figure 11. Different variations of the standard CSS process are shown. (*a*) Conductive material is deposited on the entire substrate and a resist mask is structured. (*b*) Structured electrodes after the etch step. (*c*) On chip resistor meander line, reported in [27]. (*d*) Variation without exposed dielectrics underneath the trapping zone with free hanging rf rails [93].

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

was performed to reflux the material and flatten the sharp edges. An ion trap with superconductive electrodes was fabricated using a similar process [91]. Low temperature superconductors Nb and NbN were grown onto the substrate in a sputtering step. Then the electrodes were defined using a mask and an anisotropic etch step. An annealing step was not performed after this etch step. With this variation of the standard process electroplating equipment and compatible materials are not needed to fabricate an ion trap.

A possible addition to the process was presented in [27] incorporating on-chip meander line resistors on the trap as part of the static voltage electrode filters. Bringing filters closer to the electrodes can reduce the noise induced in connecting wires as the filters are typically located outside the vacuum system or on the chip carrier. On-chip integration of trap features is essential for the future development of very large scale ion trap arrays with controls for thousands of electrodes needed for quantum computing.

In order to allow for appropriate resistance values for the resistors, processing of the chip occurs in two stages. Within the first stage only the electrode geometry is patterned with regions where resistors are to be fabricated entirely coated in photoresist. This step consists of patterning photo resist on the substrate (for example polished fused quartz [27]) to shape the electrodes followed by the deposition of the standard adhesion (0.030 μm titanium) and seed layers (0.100 μm copper) on the substrate (thicknesses stated correspond to the values used by Seidelin et al. [27]). After the electrodes have been patterned, the first mask is removed. In the next step, only the on-chip resistors are patterned allowing for different thickness of conducting layers used for resistors. A second mask is patterned on the substrate parts reserved for the on-chip resistors. Then an adhesion layer (0.013 μm titanium) and metal layer (0.030 μm gold) is deposited forming the meander lines as shown in Figure 11(*c*). The mask is removed and the rest of the sequence follows the standard process steps. This process illustrates one example for on-chip features integrated on the trap. Another process was published in [90], which integrates on-chip magnetic field coils to generate a magnetic field gradient at the trapping zone. It was fabricated using the standard process and a specific mask to form the electrodes incorporating the coils.

Most published variations [27,48,90–95] of this process feature structure sizes much smaller than achievable with the PCB process but similar to it electrodes sit directly on the substrate resulting in the same rf loss tangent requirements. It also makes the process incompatible with symmetric ion traps. As a result of the smaller structure separations, high flashover and bulk breakdown voltages are also more important. Because no slots are milled into the substrate electric charges can accumulate on the dielectrics beneath the trapping zones, which can result in stray fields and additional micromotion. To reduce this effect a high aspect ratio of electrode height to electrode–electrode distance is desirable.

Similar to the one-layer PCB process, topologies including junctions are possible but isolated electrodes

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

are prohibited by the lack of buried wires. By moving towards cleanroom fabrication techniques it is possible with this process to reduce the electrode–electrode distance and increase the trapping zone density. The scalability is still limited and the exposed dielectrics can lead to unwanted stray fields. To counter the exposed dielectrics another variation and a different process featuring 'patterned silicon on insulator (SOI) layers' can be used and will be explained in Section 6.3.

One variation of this process that prevents exposed dielectrics was fabricated by Sandia National Laboratory [93] featuring free standing rf rails with a large section of the substrate underneath the trapping region being removed. Electrodes consist of free standing wires held in place by anchor-like structures fabricated on the ends of the slot in the substrate as shown in Figure 11(*d*). To prevent snapping under stress the wires are made from connected circles increasing the flexibility. While no dielectrics are exposed the design's scalability and compatibility with different electrode geometries is limited as the rf rails are suspended between the anchors in a straight line.

6.3. *Patterned silicon on insulator layers (SOI)*

The 'Patterned Silicon on Insulator Layers' process makes use of commercially available silicon-on-insulator (SOI) substrates and was first reported by Britton et al. [49]. Similar to the PCB process this technique removes parts of a substrate instead of adding material to form the ion trap structures. Using the selective etch characteristics of the oxide layer between the two conductive silicon layers of the substrate, it is also possible to create an undercut of the dielectric and shield the ion from it, without introducing several process steps. A metal deposition step performed at the end of the process to lower the electrode resistance does not require an additional mask, keeping the number of process steps low. Therefore, this process allows for much more advanced trap structures without increasing the number of process steps by making clever use of a substrate.

The substrates are available with insulator thicknesses of up to 10 μm and different Si doping grades resulting in different resistances. After a substrate with desired characteristics (100 μm Si, 3 μm SiO_2, 540 μm Si in [49]) is found, the process sequence starts with photolithographic patterning of a mask on the top SOI silicon layer as shown in Figure 12(*a*). The mask is used to etch through the top Si layer, see Figure 12(*b*), by means of an anisotropic process (Deep Reactive Ion Etching (DRIE)). Using a wet etch process the exposed SiO_2 layer parts are removed and an undercut is formed to further reduce exposed dielectrics as shown in Figure 12(*c*). If the doping grade of the top Si layer is high enough the created structure can already be used to trap ions.

To reduce the resistance of the trap electrodes resulting from the use of bare Si a deposition step can be used to apply an additional metal coating onto the electrodes. No mask is required for this deposition step, the adhesion layer (chromium or titanium) and metal layer (1 μm gold, in [49]) can be deposited directly onto the silicon structures as shown in Figure 12(*d*). This way the electrodes and the exposed parts of the second Si layer will be coated. This has the benefit that

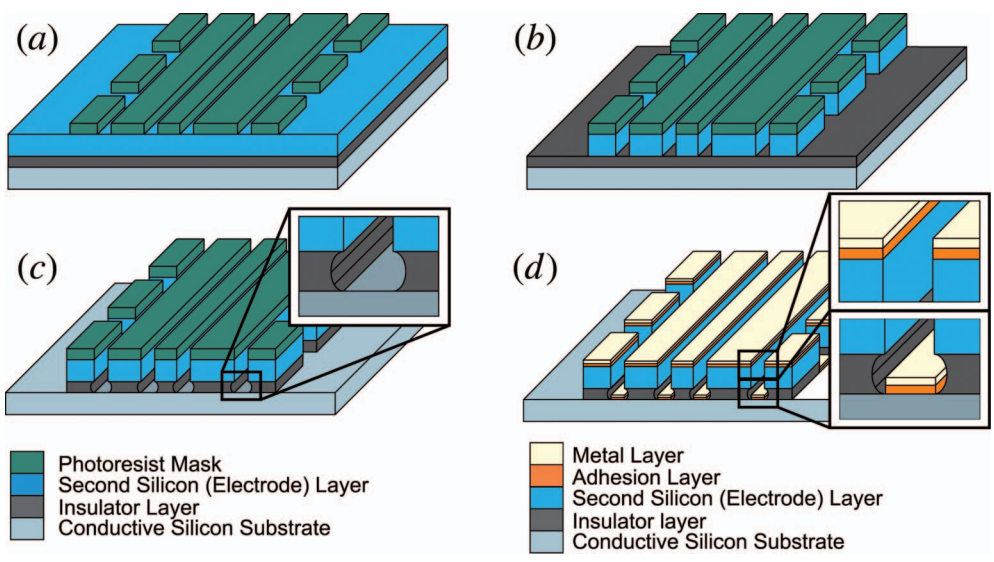


Figure 12. Fabrication sequence of the SOI process. (*a*) Resist mask is directly deposited on the substrate. (*b*) First silicon layer is etched in an anisotropic step. (*c*) Isotropic selective wet etch step removing the SiO_2 layer and creating an undercut. (*d*) Exposed Si layers coated with adhesion and conductive layer to reduce overall resistance.

possible oxidisation of the lower silicon layer is also avoided. A slot can be fabricated into the substrate underneath the trapping zone, which allows backside loading in these traps [49]. This slot is microfabricated by means of anisotropic etching using a patterned mask from the backside. The benefit of such a slot is that the atom flux needed to ionise atoms in the trapping region can be created at the backside and guided perpendicular to the trap surface away from the electrodes. Therefore, coating of the electrodes as a result of the atom flux can be minimised.

An ion trap based on the SOI process was fabricated with shielded dielectrics by Britton et al. [49]. A similar approach is used by Sterling et al. [96] to create 2D ion trap arrays. Similar to the standard CSS process, discussed in the previous section, y-junctions and other complex topologies are possible, but buried wires are prohibited. The process design incorporates a limited material choice for substrate and insulator layer. Only the doping grade of the upper and lower conductive layers can be varied not the material. The insulator layer separating the Si layers must be compatible with the SOI fabrication technique and commercially available materials are SiO_2 and Al_2O_3 (Sapphire). Adjustments of electrical characteristics, like rf loss tangent and electrode capacitances are therefore limited to the two insulator materials and geometrical variations.

To further increase the scalability and trapping zone density of ion traps, process techniques should incorporate buried wires to allow isolated static voltage and rf electrodes. Examples of such monolithic processes will be discussed next, first a process incorporating buried wires but exhibiting exposed dielectrics will be presented followed by a process allowing for buried wires and shielding of dielectrics.

6.4. *Conductive structures on insulator with buried wires (CSW)*

The process to be discussed here is a further development of the CSS process discussed in Section 6.2, which adds two more layers to incorporate buried wires. With these it is possible to connect isolated static voltage and rf electrodes and was used to fabricate an ion trap with six junctions arranged in a hexagonal shape [50], see Figure 13(*a*). The capability of buried wires is essential for more complex ion trapping arrays that could be used to trap hundreds or thousands of ions necessary for advanced quantum computing.

The process starts with the deposition of the buried conductor layer (0.300 μm gold layer [50]) sandwiched between two adhesion layers (0.02 μm titanium) on the substrate (380 μm quartz) and a patterned mask is deposited on these layers. Conductor and adhesion layers are then patterned in an isotropic etch step, see Figure 13(*b*) and then buried with an insulator material (1 μm SiO_2 deposited by means of chemical vapour deposition (CVD)). To establish contact between electrodes and the buried conductor, windows are formed in the insulator layer (plasma etching) as shown in Figure 13(*c*). Then another patterned mask is used to deposit an adhesion and conductor layer forming the electrodes (0.020 μm titanium and 1 μm gold). In this deposition step the windows in the insulator are also filled and connection between buried

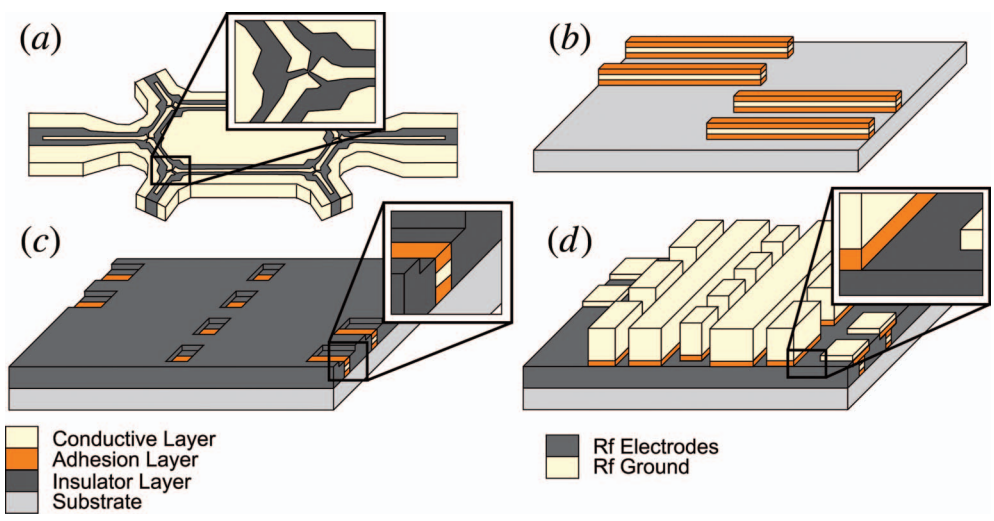


Figure 13. Process sequence for the buried wire process. (*a*) Hexagonal shaped six junction ion trap array [50]. (*b*) A structured resist mask is deposited and the mask is used to form wires in a following wet etch step. (*c*) The wires are then buried with an oxide layer and windows are formed in the oxide. (*d*) With another mask the electrodes are deposited on top of the wires and oxide layer.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

conductor and electrodes is established as shown in Figure 13(*d*). For this ion trap a backside loading slot was also fabricated using a combination of mechanical drilling and focused ion beam milling to achieve a precise slot in the substrate [50]. As demonstrated by Amini et al. [50] this process allows for large scale ion trap arrays with many electrodes and trapping zones. While the scalability is further increased, this particular process design results in exposed dielectrics. The next process improves this further by shielding the electrodes and the substrate.

6.5. *Conductive structures on insulator with ground layer (CSL)*

To achieve buried wires or in this case vertical interconnect access (vias) and shielding of dielectrics a monolithic process including a ground layer and overhanging electrodes can be carried out. Several structured and deposited layers are necessary for this process and while providing the greatest flexibility of all processes it also results in a complicated process sequence. Therefore, these processes are commonly performed using Very-Large-Scale Integration (VLSI) facilities that are capable of performing many process steps with high reliability.

A process design, which makes use of vias, was presented by Stick et al. [97]. In this process design the substrate (SOI in [97]) is coated with an insulator and a structured conductive ground layer (1 μm Al) as shown in Figure 14(*a*). This is followed by a thick structured insulator (9–14 μm). The trapping electrodes are then placed in a plane above the thick insulator. The electrodes overhang the thick insulator layer and in combination with the conductive ground layer shield the trapping zone from dielectrics. Vias are used to connect static electrodes to the conductive layer beneath the thick insulator as shown in Figure 14(*b*). The process also includes creation of a backside loading slot.

A variation from the discussed process making use of a ground plate without vias is described by Leibrandt et al. [98] and more detailed process steps are given in [93].

The described process design [97] combines vias with shielded dielectrics and also makes the trap structures independent from the substrate. Therefore, the same level of scalability as the CSW process, discussed in the previous section, can be achieved while dielectrics are shielded similar to the SOI process, described in Section 6.3. The process uses aluminium to form the electrodes which can lead to oxidisation and unwanted charge build up. To avoid this the electrodes could be coated with gold or other non-oxidising conductors in an additional step. Easier choice of substrate, isolator and electrode materials combined with vias and shielded dielectrics make this process well suited for very large scale asymmetric ion traps with high trapping zone densities and low stray fields. With electrodes in one plane and another conductive layer above the substrate this structure could also be used to fabricate a symmetric ion trap (SIT).

6.6. *Double conductor/insulator structures on substrate (DCI)*

Symmetric ion traps have electrodes placed in two or three planes with the ions trapped between the planes. Therefore, electrodes need to be precisely structured in several vertically separated layers and cannot be fabricated in one plane resulting in different requirements on the microfabrication processes. In the DCI process described here a specifically grown substrate with selective etch capabilities similar to SOI substrate layers is used and all electrodes are structured in one etch step. The first such microfabricated ion trap was created by Stick et al. [26] using this process with MBE grown AlGaAs, GaAs structures and constitutes the first realisation of a monolithic ion trap chip.

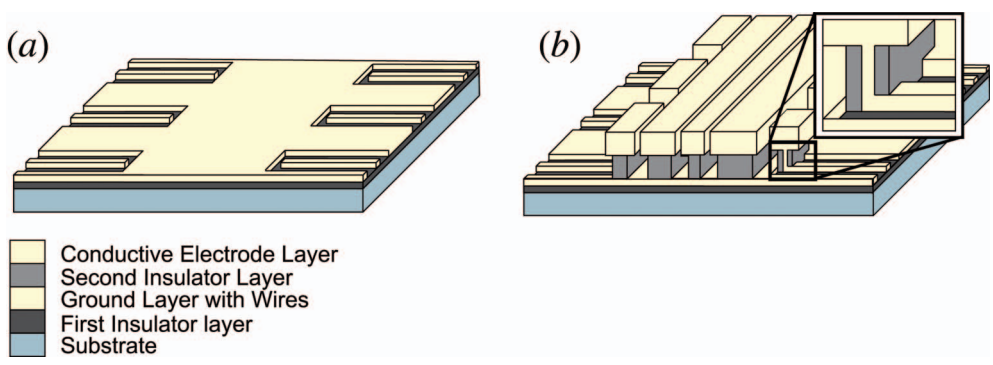


Figure 14. Two variations of the CSL process sequence. (*a*) In the process sequence published in [97] an insulating layer and a structured metal ground layer are deposited on the substrate. (*b*) Electrodes fabricated in one plane, with outer static voltage electrodes connected through vias [97].

The process starts by growing alternating layers (AlGaAs 4 μm, GaAs 2.3 μm) on a substrate using an MBE system as shown in Figure 15(*a*). The doping grades and atomic percentages (70% Al, 30% GaAs AlGaAs layer, GaAs layers highly doped 3×10^{18} cm^{-3}) are chosen to achieve low power dissipation in the electrodes. After the structure is grown a slot is etched into the substrate from the backside to allow optical access as shown in Figure 15(*b*). To provide electrical contact to both GaAs layers an anisotropic etch process is performed to remove parts of the first AlGaAs and GaAs layers, then metal is deposited onto parts of the top GaAs and the now exposed lower GaAs layer as shown in Figure 15(*c*). This is followed by an anisotropic etch step defining all the electrode structures. A following isotropic etch step creates an undercut of the insulating AlGaAs layer to increase the distance between trapping zone and dielectric, see Figure 15(*d*).

This ion trap chip could only be operated at very low rf amplitudes of 8 V as a result of the low breakdown voltage of the insulating AlGaAs material and possible residues on the insulator surfaces. This problem can be addressed by choosing a different and/or thicker insulator material.

Removing the insulator material between the electrode layers can avoid this problem almost entirely and was used in the design described by Hensinger et al. [99]. This structure is based on depositing layers instead of using a specifically grown substrate and etching material away. It incorporates a selectively etchable oxide layer, which can be completely removed after electrodes are created on this layer. This sacrificial layer allows for cantilever like electrodes without any supporting oxide layers. Therefore, breakdown can only occur over the surfaces and the capacitance between electrodes is kept at a minimum.

The process starts with the deposition of an insulating layer (Si_3N_4) on an oxidised Si substrate as shown in Figure 16(*a*). Then a conductor layer (polycrystal silicon [99]) is deposited onto the insulator and structured using an anisotropic etch process (DRIE) with a mask. Now selectively etchable sacrificial material (polysilicon glass) is deposited on the conductor structures. With a second mask windows are etched into the insulator layer allowing vertical connections to the following upper electrodes, see Figure 16(*b*). This is followed by another conductor layer (polycrystalline silicon) deposited onto the patterned insulator also filling the previously etched windows. Then an anisotropic etch is performed to structure the top conductor layer as shown in Figure 16(*c*). An etch step using a mask is then performed from the backside through the entire substrate creating a slot in the silicon substrate. With an isotropic selective hydrofluoric etch the sacrificial material used to support the polycrystal silicon electrodes during fabrication is completely removed. The electrodes now form cantilever like structures and the previously created slot in the substrate allows optical access to the trapping zone, see Figure 16(*d*).

This design potentially allows for the application of much higher voltages (breakdown for this design

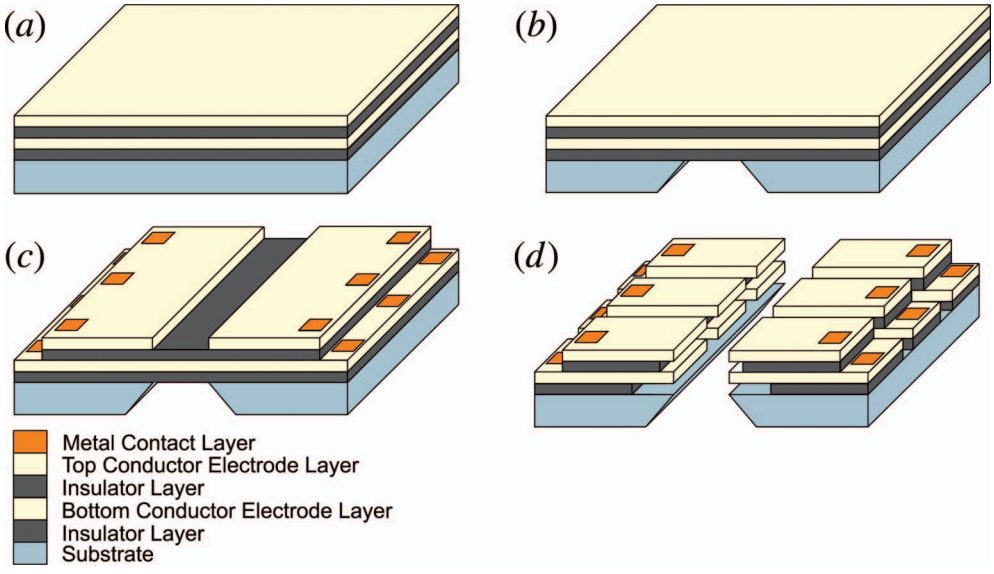


Figure 15. Fabrication process used for the symmetric trap published in [26]. (*a*) Alternately grown conductive and insulating layers on a substrate. (*b*) Backside wet etch step to allow for optical access of the trapping zone. (*c*) Structured top GaAs and AlGaAs layers, formed in an etch step using a mask. Metal contacts deposited on both electrode layers. (*d*) Structured top and bottom electrodes separated by the insulator layers and undercuts are formed by a selective wet etch.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

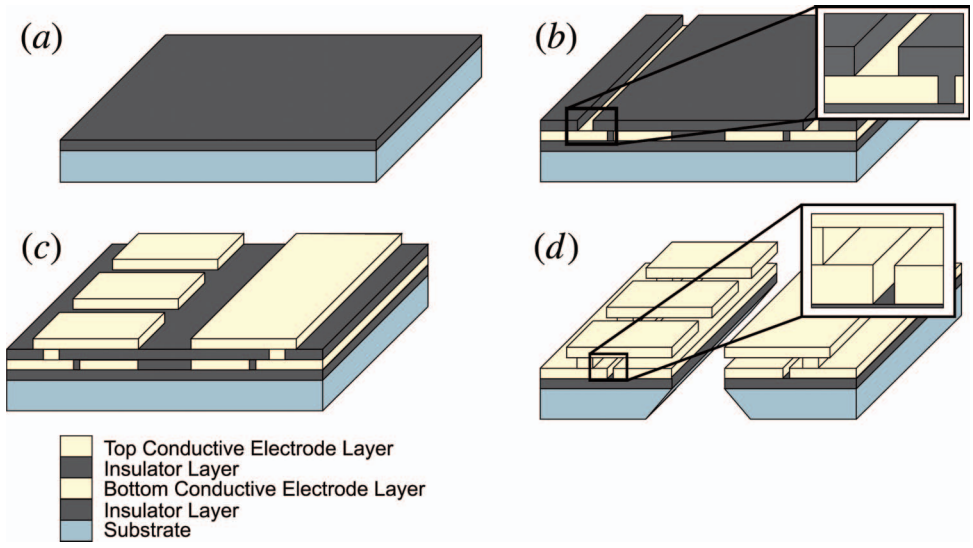


Figure 16. Process sequence for the trap proposed in [99]. (*a*) Insulator layer deposited on the substrate. (*b*) Structured electrode conductor layer and a second selectively etchable insulator is deposited and structured. (*c*) The second conductor layer is deposited, making a vertical electrical connection to the lower conductor layer and is structured using an anisotropic etch process. (*d*) All selectively etchable insulator layers are removed and a backside etch is performed creating a slot in the substrate.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

would occur over an insulator surface rather than through insulator bulk).

Independent of the material, the distance between the two electrode planes is limited by the maximal allowable insulator thickness which is often determined by particular deposition and etch constraints. To keep the ion–electrode distance at a desired level the aspect ratio of horizontal and vertical electrode–electrode distances (see Figure 16(*d*)) has to be much higher than one. As described in Section 3.1 this leads to a low geometric efficiency factor η and reduces the trap depths and secular frequencies of these traps. By forming the electrodes on the upper and lower side of an oxidised substrate this aspect ratio can be dramatically decreased. A process technique following this consideration will be discussed next.

6.7. *Double conductor structures on oxidised silicon substrate (DCS)*

In this proposed monolithic process [100] an oxidised silicon substrate separates the electrode structures, which allows for much higher electrode to electrode distances. Making use of both sides of the substrate separates this process from all other described techniques. It allows electrode–electrode distances of hundreds of micrometres, which would otherwise be impossible due to maximal thicknesses of deposited or grown oxide layers. Therefore, a ratio of one for the horizontal and vertical electrode–electrode distances can be achieved, resulting in an optimal geometric efficiency factor η. The trap is fabricated in several process steps starting with the oxidisation of a silicon wafer. Using an anisotropic etch process and a patterned mask, slots are then formed in the SiO_2 layers on both sides exposing the Si wafer and creating the future trenches between electrodes as shown in Figure 17(*a*). Then conductive layers are deposited on both sides of the wafer forming the two electrode layers. The individual electrodes are then created on both sides in an anisotropic etch step using a patterned mask as shown in Figure 17(*b*). This is followed by an isotropic wet etch through the silicon using another mask resulting in an under cut of the electrodes and providing the optical access as shown in Figure 17(*c*). The now exposed dielectric SiO_2 layers are then coated in a shadow metal evaporation process and the remaining mask is removed. After all conductor layers are deposited, the layer thickness is increased by means of electroplating resulting in the final structure shown in Figure 17(*d*) [100]. By using the entire substrate to separate the electrodes this proposed process sequence allows for a low aspect ratio of horizontal and vertical electrode–electrode distance. All electrodes sit on a dielectric material increasing the importance of a low rf loss tangent of the insulating SiO_2 layers.

6.8. *Assembly of precision machined structures (PMS)*

Non-monolithic fabrication processes are commonly based on the assembly of pre-structured parts, using techniques like wafer bonding or mechanical clamping. The scalability of non-monolithic processes can be

limited due to this and therefore are commonly used for ion traps with only one or a few trapping zones. Systems with thousands of isolated electrodes would be difficult to realise with a non-monolithic process. Advantages of the non-monolithic processes are a greater choice of materials used and fabrication techniques, ranging from machined metal structures over laser machined alumina, to structured Si substrates.

A non-monolithic process can be based on the assembly of precision machined structures commonly done in workshops and will not be discussed in detail. Two examples for ion traps fabricated with this process are the needle trap with needle tip radius of approximately 3 μm reported by Deslauriers et al. [101] and a blade trap used by McLoughlin et al. in [52]. More complex ion trap geometries including junctions and more electrodes can also be realised with non-monolithic processes and will therefore be discussed next.

6.9. *Assembly of laser machined alumina structures (LMA)*

Trap structures can be created by precision laser machining and coating of alumina substrates and mechanically assembling these using spacers and clamps as shown in Figure 18. The structures are created by laser machining slots into an alumina substrate resulting in cantilevers providing the mechanical stability for the electrodes, see Figure 18(*a*). The alumina cantilevers are then coated with a conductive layer, commonly metal, to form the electrodes. To prevent electrical shorting between the electrodes a patterned mask is used during this step. Several structured and coated

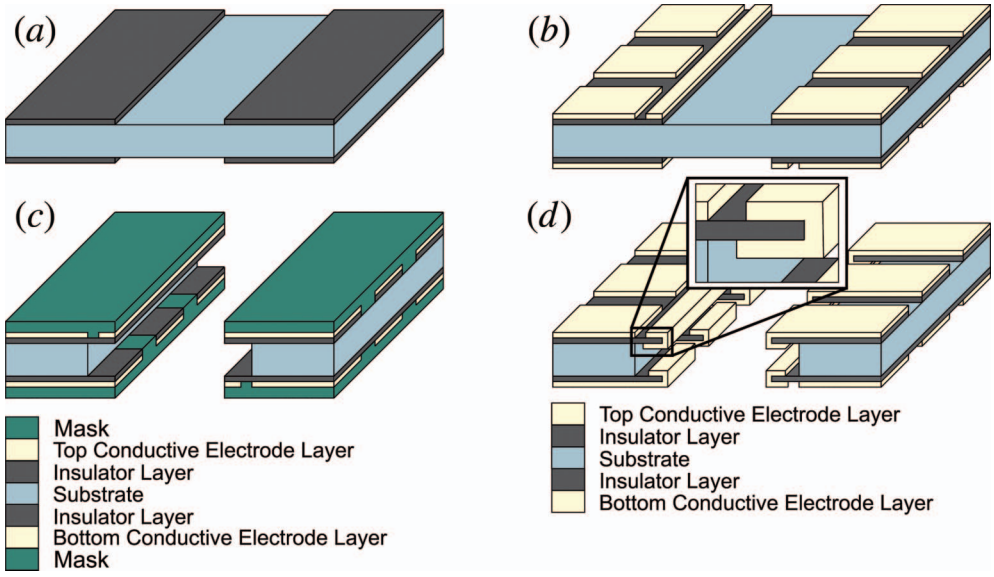


Figure 17. Process sequence as used by Brownnutt et al. [100]. (*a*) A structured insulator layer is deposited on both sides of the substrate. (*b*) Electrode structures are then deposited on this insulator layer. (*c*) Parts of the insulator are also removed in this step and a slot is etched into the substrate. The top and bottom structures are then covered with a mask. (*d*) Shadow evaporation is used to coat exposed dielectrics close to the trapping zone. The mask is removed and the conductor layer thickness increased by means of electroplating.

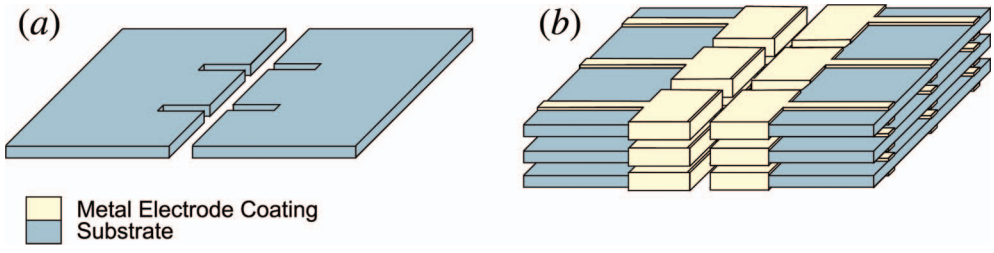


Figure 18. 'Assembly of Laser Machined Alumina structures' process sequence. (*a*) Cantilever like structures are formed in the alumina structures using a laser. (*b*) Parts of the substrate are coated using a mask forming the electrodes and electrical connections. Three similar layers are mounted on top of each other to form a three-layer symmetric trap.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

alumina plates are then mechanically assembled to form a two or three layer trap [28,29,102]. Normally spacers are used to maintain an exact distance between the plates, which are then exactly positioned and held in place using mechanical pressure, see Figure 18(*b*).

One of the first ion traps with linear sections using this process was reported by Turchette et al. [102]. Another example of such a trap was used for the first demonstration of corner shuttling of ions within a two-dimensional ion trap array [28]. Other traps fabricated with this process include the trap used for near adiabatic shuttling through a junction [29] and the traps reported in [103,104]. The necessary alumina substrates show a small loss tangent. A similar non-monolithic process based on clean room fabrication techniques, which allows for higher precision and greater choice of substrate material, will be discussed next.

6.10. Wafer bonding of lithographic structured semiconductor substrates (WBS)

This process technique is similar to the monolithic SOI substrate technique discussed in Section 6.3 creating a highly doped conductor on an insulator using wafer bonding techniques. Much higher insulator thicknesses can be achieved with this process and many types of insulator and substrates can be used. This process was used to fabricate symmetric and asymmetric ion traps.

First a process used for an asymmetric ion trap will be discussed, starting with a commercially available substrate (Si wafer, resistivity $= 500 \times 10^{-6}\ \Omega$ cm). Using anisotropic etching with a patterned mask (DRIE) the wafer is structured. All electrodes are physically connected outside the trapping zone to provide the necessary stability during the fabrication as shown in Figure 19(*a*). The structured substrate is then bonded on another substrate with a sandwiched and structured insulator layer providing electrical insulation and mechanical stability as shown in Figure 19(*b*). In the insulator layer a gap is formed underneath the trapping region leaving no exposed dielectrics underneath the ion. The bonding also provides the needed structural stability and the physical connections between the electrodes can then be removed by dicing the substrate, Figure 19(*b*). Similar to the SOI substrate process a conductive layer can be deposited on top of the structured substrate. A patterned mask is not necessary and the conductive layer can be directly deposited. Depending on the material used and substrate an adhesion layer has to be added.

Another variation of this process can be used to fabricate symmetric ion traps. Both substrates are identically structured and wafer bonded. An additional etch step is introduced to make the substrate thinner adjacent to the trapping zone in order to improve optical access as shown in Figure 19(*c*). Similar to the asymmetric trap, the parts are then wafer bonded together with a sandwiched insulator layer Figure 19(*d*). When used for asymmetric traps the dielectrics are completely shielded from the trapping zone and for the case of symmetric traps the dielectrics can be placed far away from the trapping zone. Possible geometries

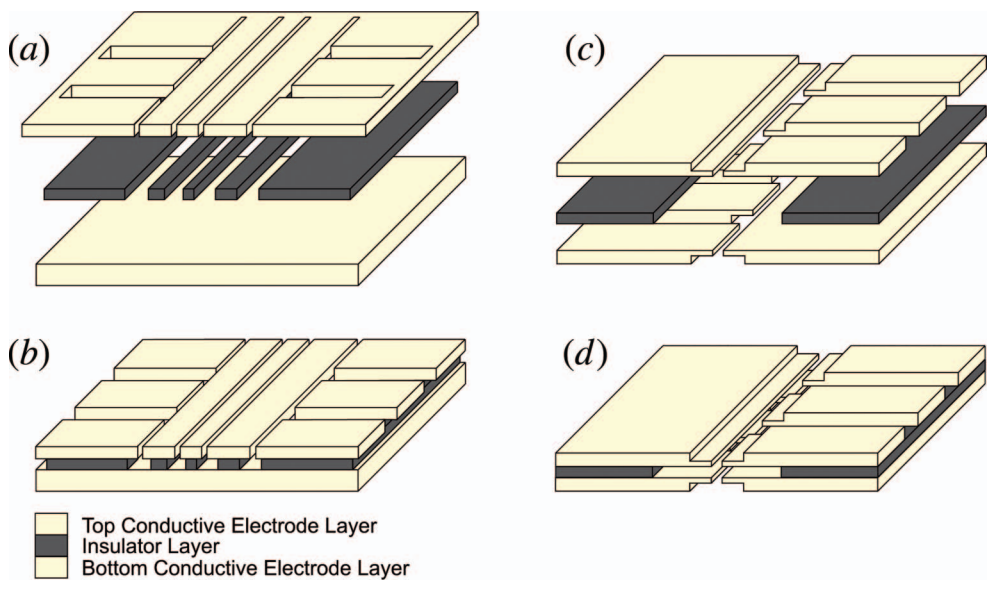


Figure 19. Processes used to fabricate symmetric and asymmetric non-monolithic ion traps via waver bonding. (*a*) Microfabricated structures used for the assembly of an asymmetric trap. The structures are still physically connected within each layer. (*b*) These parts are then waferbonded together and physical connections are removed forming the trap structure. (*c*) Microfabricated parts used for a symmetric trap. (*d*) Waferbonded parts creating a symmetric trap.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

for asymmetric ion traps are limited with this technique as buried wires and therefore isolated electrodes are not possible. The fabrication method and choice of electrode materials used for this trap can result in a very low surface roughness of less than 1 nm.

7. Anomalous heating

One limiting factor in producing smaller and smaller ion traps is motional heating of trapped ions. While it only has limited impact in larger ion traps it becomes more important when scaling down to very small ion–electrode distances. The most basic constraint is to allow for laser cooling of the ion. If the motional heating rate is of similar magnitude as the photon scattering rate, laser cooling is no longer possible. Therefore, for most applications, the ion–electrode distance should be chosen so the expected motional heating rate is well below the photon scattering rate. Depending on the particular application, there may be more stringent constraints. For example, in order to realise high fidelity quantum gates that rely on motional excitation for entanglement creation of internal states [105,106], motional heating should be negligible on the time scale of the quantum gate. This timescale is typically related to the secular period $1/\omega_m$ of the ion motion, however, it can also be faster [107]. Motional heating of trapped ions in an ion trap is caused by fluctuating electric fields (typically at the secular frequency of the ion motion). These electric fields originate from voltage fluctuations on the ion trap electrodes. One would expect some voltage fluctuations from the electrodes due to the finite impedance of the trap electrodes, this effect is known as Johnson noise. Resulting heating would have a $1/d^2$ scaling [102] where d is the characteristic nearest ion–electrode distance. However, in actual experiments a much larger heating rate has been observed. In fact, heating measurements taken for a variety of ions and ion trap materials seem to loosely imply a $1/d^4$ dependence of the motional heating rate $\dot{\bar{n}}$. A mechanism beyond Johnson noise must be responsible for this heating and this mechanism was termed 'anomalous heating'. In order to establish a more reliable scaling law, an experiment was carried out where the heating rate of an ion trapped between two needle electrodes was measured [101]. The experimental setup allowed for controlled movement of the needle electrodes. It was therefore possible to vary the ion–electrode distance and an experimental scaling law was measured $\dot{\bar{n}} \sim 1/d^{3.5\pm0.1}$ [101]. The motional heating of the secular motion of the ion can be expressed as [102]

$$\dot{\bar{n}} = \frac{q^2}{4m\hbar\omega_m}\left(S_E(\omega_m) + \frac{\omega_m^2}{2\Omega_T^2}S_E(\Omega_T \pm \omega_m)\right). \quad (17)$$

ω_m is the secular frequency of the mode of interest, typically along the axial direction of the trap, Ω_T is the drive frequency and the power spectrum of the electric field noise is defined as $S_E(\omega) = \int_{-\infty}^{\infty}\langle E(\tau)\, E(t+\tau)\rangle \exp(\mathrm{i}\omega\tau)\,\mathrm{d}\tau$. The second term represents the cross-coupling between the noise and rf fields and can be neglected for axial motion in linear traps as the axial confinement is only produced via static fields [15,102].

A model was suggested to explain the $1/d^4$ trend that considered fluctuating patch potentials; a large number of randomly distributed 'small' patches on the inside of a sphere, where the ion sits at centre at a distance d [102]. All patches have a power noise spectral density that influence the electric field at the ion position, over which is averaged to eventually deduce the heating rate. Figure 20 shows a collection of published motional heating results. Instead of plotting the actual heating rate, we plot the spectral noise density $S_E\ (\omega_m)$ multiplied with the secular frequency in order to scale out behaviour from different ion mass or different secular frequencies used in individual experiments. We also plot a $1/d^4$ trend line. We note that previous experiments [52,101] consistently showed $S_E\ (\omega_m) \sim 1/\omega_m$ allowing the secular frequency to be scaled out by plotting $S_E\ (\omega_m) \times \omega_m$ rather than just $S_E\,(\omega_m)$. In the experiment by Deslauriers et al. [101], another discovery was made. The heating rate was found to be massively suppressed by mild cooling of the trap electrodes. Cooling the ion trap from 300 K down to 150 K reduced the heating by an order of magnitude [101]. This suggests the patches are thermally activated. Labaziewicz et al. [92] measured motional heating for temperatures as low as 7 K and found a multiple-order-of-magnitude reduction of motional heating at low temperatures. The same group measured a scaling law for the temperature dependence of the spectral noise density for a particular ion trap as $S_E\,(T) = 42(1 + (T/46K)^{4.1}) \times 10^{-15}\ \mathrm{V^2\ m^{-2}\ Hz^{-1}}$ [94]. Superconducting ion traps consisting of niobium and niobium nitride were tested above and below the critical temperature T_c and showed no significant change in heating rate between the two states [91]. Within the same study, heating rates were reported for gold and silver trap electrodes at the same temperature (6 K) showing no significant difference between the two and superconducting electrodes. This suggests that anomalous heating is mainly caused by noise sources on the surfaces, although the exact cause of anomalous heating is not yet fully understood. From the information available, it is likely that surface properties play a critical role, however, other factors such as material bulk properties, oxide layers may also play an important role and much more work is still needed to

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

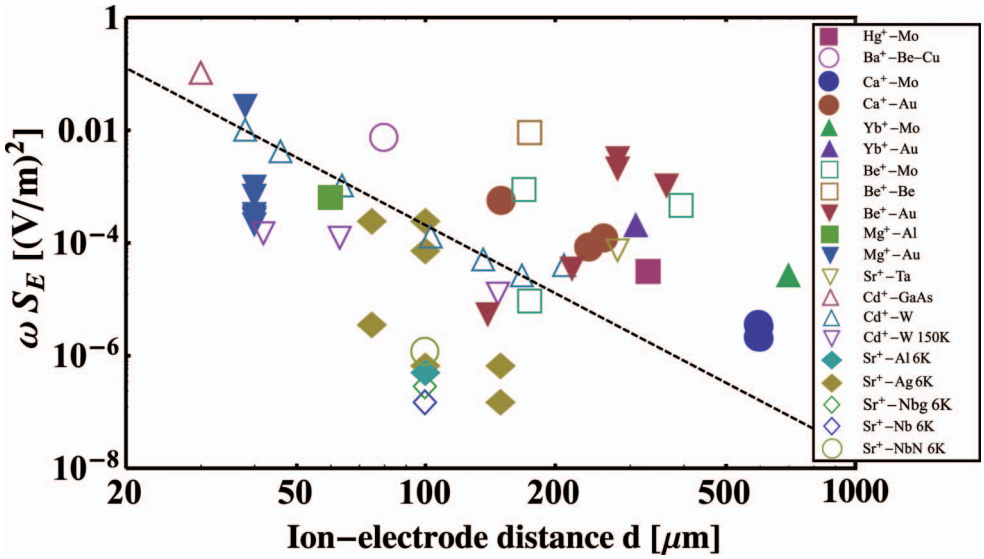


Figure 20. Previously published measurements of motional heating plotted as the product of electric field noise spectral density $S_E(\omega)$ and the secular frequency ω, versus ion–electrode distance d. A $1/d^4$ trend line is also shown. Each label shows both the ion species and the electrode material used and the electrode temperature is also noted if the measurement is performed below room temperature. The data point are associated with the following references (Hg^+-Mo [108], Ba^+-Be–Cu [109], Ca^+-Mo [110], Ca^+-Au [48, 104, 111], Yb^+-Mo [112], Yb^+-Au [52], Be^+ − Mo [102], Be^+-Be [102], Be^+-Au [102, 103], Mg^+-Al [113], Mg^+-Au [27, 49, 50, 113, 114], Sr^+-Ta [115], Cd^+-GaAs [26], Cd^+-W [101], Cd^+-W 150 K [101], Sr^+-Al 6 K [91], Sr^+-Ag 6 K [92], Sr^+-Nbg 6 K, Sr^+-Nb 6 K, Sr^+-NbN 6 K [91]).

fully understand and control anomalous heating. While anomalous heating limits our ability to make extremely small ion traps, it does not prevent the use of slightly larger microfabricated ion traps. Learning how to mitigate anomalous heating is therefore not a prerequisite for many experiments, however, mitigating it will help to increase experimental fidelities (such as in quantum gates) and will allow for the use of smaller ion traps.

8. Conclusion

Microfabricated ion traps provide the opportunity for significant advances in quantum information processing, quantum simulation, cavity QED, quantum hybrid systems, precision measurements and many other areas of modern physics. We have discussed the basic principles of microfabricated ion traps and highlighted important factors when designing such ion traps. We have discussed important electrical and material considerations when scaling down trap dimensions. We presented a detailed overview of a vast range of ion trap geometries and showed how they can be fabricated using different fabrication processes employing advanced microfabrication methods. A limiting factor to scaling down trap dimensions even further is motional heating in ion traps and we have summarised current knowledge of its nature and how it can be mitigated. The investigation of microfabricated ion traps lies on the interface of atomic physics and state-of-the-art nanoscience. This is a very young research field with room for many step-changing innovations. In addition to the development of trap structures themselves, future research will focus on advanced on-chip features such as cavities, electronics, digital signal processing, fibres, waveguides and other integrated functionalities. Eventually progress in this field will result in on-chip architectures for next generation quantum technologies allowing for the implementation of large scale quantum simulations and quantum algorithms. The inherent scalability of such condensed matter systems coupled with the provision of atomic qubits which are highly decoupled from the environment will allow for ground-breaking innovations in many areas of modern physics.

Acknowledgements

We acknowledge the support by the UK Engineering and Physical Sciences Research Council (EP/E011136/1, EP/G007276/1), the European Commission's Sixth Framework Marie Curie International Reintegration Programme (MIRG-CT-2007-046432), the Nuffield Foundation and the University of Sussex.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

Notes on contributors

Marcus Hughes gained his MPhys Physics at the University of Sussex in 2008 and has carried on studying for his D.Phil. within the Sussex Ion Quantum Technology group. His interests include quantum information and microfabricated ion traps.

Bjoern Lekitsch is a D.Phil. student at the University of Sussex in the Ion Quantum Technology group. He completed his Dipl. Ing. degree in Nanostrukturtechnik at the Physics Department at the University of Wuerzburg, Germany in 2010. His interests include quantum information technology, microfabrication of ion traps and shuttling of ions trough optimised junctions in large ion traps arrays.

Jiddu Broersma, a University of Sussex graduate student obtained his MPhys Theoretical Physics in 2010. He completed his final year research project in the Sussex Ion Quantum Technology group. His interests include quantum information science, neural networks and renewable energies.

Winfried Hensinger is a Reader in Quantum, Atomic and Optical Physics and heads the Ion Quantum Technology group at the University of Sussex. In 2008 he was awarded an EPSRC Leadership fellowship for the development of quantum technology with nanofabricated ion trap chips. He obtained his undergraduate degree at the Ruprechts-Karls University in Heidelberg, Germany and his Ph.D. at the University of Queensland in Brisbane, Australia studying experimental quantum nonlinear dynamics with ultracold atoms. During his Ph.D. candidature he spent an extended period at the National Institute of Standards and Technology in Gaithersburg, USA where he demonstrated dynamical tunnelling in a Bose–Einstein condensate. After completing his Ph.D. he spent 3 years as a FOCUS Research Fellow at the University of Michigan, USA, working on scalable quantum information processing with trapped ions. He developed the first monolithic ion trap chip and demonstrated the first experimental realisation of a two-dimensional ion trap array where individual ions can be shuttled around corners. His primary research direction is the development of quantum technologies beyond proof-of-principle.

References

[1] W. Paul, *Electromagnetic traps for charged and neutral particles*, Rev. Mod. Phys. 62 (1990), pp. 531–540.

[2] H.G. Dehmelt, *Radiofrequency spectroscopy of stored ions I: Storage*, Adv. At. Mol. Phys. 3 (1967), p. 53.

[3] M. Keller, B. Lange, K. Hayasaka, W. Lange, and H. Walther, *Deterministic cavity quantum electrodynamics with trapped ions*, J. Phys. B: At. Mol. Opt. Phys. 36 (2003), pp. 613–622.

[4] P.F. Herskind, A. Dantan, J.P. Marler, M. Albert, and M. Drewsen, *Realization of collective strong coupling with ion Coulomb crystals in an optical cavity*, Nature Phys. 5 (2009), pp. 494–498.

[5] M. Pons, V. Ahufinger, C. Wunderlich, A. Sanpera, S. Braungardt, A. Sen(De), U. Sen, and M. Lewenstein, *Trapped ion chain as a neural network: error resistant quantum computation*, Phys. Rev. Lett. 98 (2007), 023003.

[6] A. Friedenauer, H. Schmitz, J.T. Glueckert, D. Porras, and T. Schaetz, *Simulating a quantum magnet with trapped ions*, Nature Phys. 4 (2008), pp. 757–761.

[7] M. Johanning, A.F. Varón, and C. Wunderlich, *Quantum simulations with cold trapped ions*, J. Phys. B 42 (2009), 154009.

[8] R.J. Clark, T. Lin, K.R. Brown, and I.L. Chuang, *A two-dimensional lattice ion trap for quantum simulation*, J. Appl. Phys. 105 (2009), 013114.

[9] K. Kim, M.S. Chang, S. Korenblit, R. Islam, E.E. Edwards, J.K. Freericks, G.D. Lin, L.M. Duan, and C. Monroe, *Quantum simulation of frustrated Ising spins with trapped ions*, Nature 465 (2010), pp. 590–593.

[10] T. Udem, S.A. Diddams, K.R. Vogel, C.W. Oates, E.A. Curtis, W.D. Lee, W.M. Itano, R.E. Drullinger, J.C. Bergquist, and L. Hollberg, *Absolute frequency measurements of the Hg^+ and Ca optical clock transitions with a femtosecond laser*, Phys. Rev. Lett. 86 (2001), pp. 4996–4999.

[11] S.A. Webster, P. Taylor, M. Roberts, G.P. Barwood, and P. Gill, *Kilohertz-resolution spectroscopy of the $^2S_{1/2}-{}^2F_{7/2}$ electric octupole transition in a single $^{171}Yb^+$ ion*, Phys. Rev. A 65 (2002), 052501.

[12] C. Tamm, S. Weyers, B. Lipphardt, and E. Peik, *Stray-field-induced quadrupole shift and absolute frequency of the 688-THz $^{171}Yb^+$ single-ion optical frequency standard*, Phys. Rev. A 80 (2009), 043403.

[13] M. Chwalla, J. Benhelm, K. Kim, G. Kirchmair, T. Monz, M. Riebe, P. Schindler, A.S. Villar, W. Hänsel, C.F. Roos, R. Blatt, M. Abgrall, G. Santarelli, G.D. Rovera, and P. Laurent, *Absolute frequency measurement of the $^{40}Ca^+$ $4s^2S_{1/2} - 3d^2D_{5/2}$ clock transition*, Phys. Rev. Lett. 102 (2009), 023002.

[14] J.I. Cirac and P. Zoller, *Quantum computations with cold trapped ions*, Phys. Rev. Lett. 74 (1995), pp. 4091–4094.

[15] D.J. Wineland, C. Monroe, W.M. Itano, D. Leibfried, B.E. King, and D.M. Meekhof, *Experimental issues in coherent quantum-state manipulation of trapped atomic ions*, J. Res. Nat. Inst. Stand. Tech. 103 (1998), pp. 259–328.

[16] H. Häffner, C.F. Roos, and R. Blatt, *Quantum computing with trapped ions*, Phys. Rep. 469 (2008), pp. 155–203.

[17] D.P. DiVincenzo, *Quantum computation*, Science 270 (1995), pp. 255–261.

[18] D. Leibfried, D.M. Meekhof, B.E. King, C. Monroe, W.M. Itano, and D.J. Wineland, *Experimental determination of the motional quantum state of a trapped atom*, Phys. Rev. Lett. 77 (1996), pp. 4281–4285.

[19] D. Leibfried, D.M. Meekhof, B.E. King, C. Monroe, W.M. Itano, and D.J. Wineland, *Experimental preparation and measurement of quantum states of motion of a trapped atom*, J. Mod. Opt. 44 (1997), p. 2485.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

[20] D. Leibfried, B. DeMarco, V. Meyer, D. Lucas, M. Barrett, J. Britton, W.M. Itano, B. Jelenkovic, C. Langer, T. Rosenband, and D.J. Wineland, *Experimental demonstration of a robust, high-fidelity geometric two ion-qubit phase gate*, Nature 422 (2003), pp. 412–415.

[21] A. Sørensen and K. Mølmer, *Quantum computation with ions in thermal motion*, Phys. Rev. Lett. 82 (1999), pp. 1971–1974.

[22] J. Benhelm, G. Kirchmair, C.F. Roos, and R. Blatt, *Towards fault-tolerant quantum computing with trapped ions*, Nature Phys. 4 (2008), pp. 463–466.

[23] D.M. Lucas, B.C. Keitch, J.P. Home, G. Imreh, M.J. McDonnell, D.N. Stacey, D.J. Szwer, and A.M. Steane, *A long-lived memory qubit on a low-decoherence quantum bus*, preprint (2007). Available at arXiv:0710.4421v1.

[24] A.H. Myerson, D.J. Szwer, S.C. Webster, D.T.C. Allcock, M.J. Curtis, G. Imreh, J.A. Sherman, D.N. Stacey, A.M. Steane, and D.M. Lucas, *High-fidelity readout of trapped-ion qubits*, Phys. Rev. Lett. 100 (2008), 200502.

[25] M. Acton, K.A. Brickman, P. Haljan, P. Lee, L. Deslauriers, and C. Monroe, *Near-perfect simultaneous measurement of a qubit register*, Quantum Inf. Comp. 6 (2006), pp. 465–482.

[26] D. Stick, W.K. Hensinger, S. Olmschenk, M.J. Madsen, K. Schwab, and C. Monroe, *Ion trap in a semiconductor chip*, Nature Phys. 2 (2006), pp. 36–39.

[27] S. Seidelin, J. Chiaverini, R. Reichle, J.J. Bollinger, D. Leibfried, J. Britton, J.H. Wesenberg, R.B. Blakestad, R.J. Epstein, D.B. Hume, W.M. Itano, J.D. Jost, C. Langer, R. Ozeri, N. Shiga, and D.J. Wineland, *Microfabricated surface-electrode ion trap for scalable quantum information processing*, Phys. Rev. Lett. 96 (2006), 253003.

[28] W.K. Hensinger, S. Olmschenk, D. Stick, D.H. Hucul, M. Yeo, M. Acton, L. Deslauriers, and C. Monroe, *T-junction ion trap array for two-dimensional ion shuttling, storage, and manipulation*, Appl. Phys. Lett. 88 (2006), 034101.

[29] R.B. Blakestad, C. Ospelkaus, A.P. VanDevender, J.M. Amini, J. Britton, D. Leibfried, and D.J. Wineland, *High-fidelity transport of trapped-ion qubits through an X-junction trap array*, Phys. Rev. Lett. 102 (2009), 153002.

[30] J.I. Cirac and P. Zoller, *A scalable quantum computer with ions in an array of microtraps*, Nature 404 (2000), pp. 579–581.

[31] D. Kielpinski, C. Monroe, and D. Wineland, *Architecture for a large-scale ion-trap quantum computer*, Nature 417 (2002), pp. 709–711.

[32] A. Steane, *The ion trap quantum information processor*, Appl. Phys. B 64 (1997), pp. 623–642.

[33] R.C. Thompson, S. Donnellan, D.R. Crick, and D.M. Segal, *Applications of laser cooled ions in a Penning trap*, J. Phys. B: At. Mol. Opt. Phys. 42 (2009), 154003.

[34] J.R. Castrejón-Pita, H. Ohadi, D.R. Crick, D.F.A. Winters, D.M. Segal, and R.C. Thompson, *Novel designs for Penning ion traps*, J. Mod. Opt. 54 (2007), pp. 1581–1594.

[35] W. Paul, *Electromagnetic traps for charged and neutral particles*, Rev. Mod. Phys. 62 (1990), pp. 531–540.

[36] P.K. Ghosh, *Ion Traps*, Oxford University Press, New York, 1995.

[37] G.Z.K. Horvath, R.C. Thompson, and P.L. Knight, *Fundamental physics with trapped ions*, Contemp. Phys. 38 (1997), pp. 25–48.

[38] R.C. Thompson, *Spectroscopy of trapped ions*, Adv. At. Mol. Phys. 31 (1993), pp. 63–136.

[39] D.J. Griffiths, *Introduction to Electrodynamics*, 3rd ed., Benjamin Cummings, San Francisco, 1999.

[40] F.M. Penning, *Die Glimmentladung bei niedrigem Druck zwischen koaxialen Zylindern in einem axialen Magnetfeld*, Physica 3 (1936), pp. 873–894.

[41] M. Abramowitz and I.A. Stegun, *Handbook of Mathematical Functions*, Dover Publications, New York, 1965.

[42] M.J. Madsen, W.K. Hensinger, D. Stick, J.A. Rabchuk, and C. Monroe, *Planar ion trap geometry for microfabrictaion*, Appl. Phys. B (2004), pp. 639–651.

[43] D.J. Berkeland, J.D. Miller, J.C. Bergquist, W.M. Itano, and D.J. Wineland, *Minimization of ion micromotion in a Paul trap*, J. Appl. Phys. 83 (1998), pp. 5025–5033.

[44] A. Steane, C.F. Roos, D. Stevens, A. Mundt, D. Leibfried, F. Schmidt-Kaler, and R. Blatt, *Speed of ion-trap quantum-information processors*, Phys. Rev. A 62 (2000), 042305.

[45] D. Hucul, M. Yeo, W.K. Hensinger, J. Rabchuk, S. Olmschenk, and C. Monroe, *On the transport of atomic ions in linear and multidimensional ion trap arrays*, Quantum Inf. Comput. 8 (2008), pp. 501–578.

[46] C. Monroe, D.M. Meekhof, B.E. King, S.R. Jefferts, W.M. Itano, D.J. Wineland, and P. Gould, *Resolved-sideband Raman cooling of a bound atom to the 3D zero-point energy*, Phys. Rev. Lett. 75 (1995), pp. 4011–4014.

[47] B.E. King, C.S. Wood, C.J. Myatt, Q.A. Turchette, D. Leibfried, W.M. Itano, C. Monroe, and D.J. Wineland, *Cooling the collective motion of trapped ions to initialize a quantum register*, Phys. Rev. Lett. 81 (1998), pp. 1525–1528.

[48] D.T.C. Allcock, J.A. Sherman, D.N. Stacey, A.H. Burrell, M.J. Curtis, G. Imreh, N.M. Linke, D.J. Szwer, S.C. Webster, A.M. Steane, and D.M. Lucas, *Implementation of a symmetric surface-electrode ion trap with field compensation using a modulated Raman effect*, New J. Phys. 12 (2010), 053026.

[49] J. Britton, D. Leibfried, J.A. Beall, R.B. Blakestad, J.H. Wesenberg, and D.J. Wineland, *Scalable arrays of rf Paul traps in degenerate Si*, Appl. Phys. Lett. 95 (2009), 173102.

[50] J.M. Amini, H. Uys, J.H. Wesenberg, S. Seidelin, J. Britton, J.J. Bollinger, D. Leibfried, C. Ospelkaus, A.P. VanDevender, and D.J. Wineland, *Toward scalable ion traps for quantum information processing*, New J. Phys. 12 (2010), 033031.

[51] A.H. Nizamani and W.K. Hensinger, *Optimum electrode configurations for fast ion separation in microfabricated surface ion traps*, preprint (2010), to appear in Appl. Phys. B. Available at arXiv:1007.3542v2.

[52] J.J. McLoughlin, A.H. Nizamani, J.D. Siverns, R.C. Sterling, M.D. Hughes, B. Lekitsch, B. Stein, S. Weidt, and W.K. Hensinger, *Versatile ytterbium ion trap experiment for operation of scalable ion-trap chips with motional heating and transition-frequency measurements*, Phys. Rev. A 83 (2011), 013406.

[53] J.D. Siverns, L.R. Simkins, S. Weidt, and W.K. Hensinger, *On the application of radio frequency voltages to ion traps via helical resonators*, preprint (2011). Available at arXiv:1106.5013v1.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

[54] L. Deslauriers, M. Acton, B.B. Blinov, K.A. Brickman, P.C. Haljan, W.K. Hensinger, D. Hucul, S. Katnik, R.N. Kohn, P.J. Lee, M.J. Madsen, P. Maunz, S. Olmschenk, D.L. Moehring, D. Stick, J. Sterk, M. Yeo, K.C. Younge, and C. Monroe, *Efficient photoionization loading of trapped ions with ultrafast pulses*, Phys. Rev. A 74 (2006), 063421.

[55] J. Britton, D. Leibfried, J.A. Beall, R.B. Blakestad, J.J. Bollinger, J. Chiaverini, R.J. Epstein, J.D. Jost, D. Kielpinski, C. Langer, R. Ozeri, R. Reichle, S. Seidelin, N. Shiga, J.H. Wesenberg, and D.J. Wineland, *A microfabricated surface-electrode ion trap in silicon*, preprint (2008). Available at arXiv:quant-ph/0605170v1.

[56] J.H. Wesenberg, *Ideal intersections for radio-frequency trap networks*, Phys. Rev. A 79 (2009), 013416.

[57] F. Splatt, M. Harlander, M. Brownnutt, F. Zaehringer, R. Blatt, and W. Haensel, *Deterministic reordering of 40Ca+ ions in a linear segmented Paul trap*, New J. Phys. 11 (2009), 103008.

[58] R. Reichle, D. Leibfried, R.B. Blakestad, J. Britton, J.D. Jost, E. Knill, C. Langer, R. Ozeri, S. Seidelin, and D.J. Wineland, *Transport dynamics of single ions in segmented microstructured Paul trap arrays*, Fortschr. Phys. 54 (2006), pp. 666–685.

[59] K. Singer, U. Poschinger, M. Murphy, P. Ivanov, F. Ziesel, T. Calarco, and F. Schmidt-Kaler, *Colloquium: Trapped ions as quantum bits: Essential numerical tools*, Rev. Mod. Phys. 82 (2010), pp. 2609–2632.

[60] M.H. Oliveira and J.A. Miranda, *Biot-Savart-like law in electrostatics*, Eur. J. Phys. 22 (2001), pp. 31–38.

[61] J.H. Wesenberg, *Electrostatics of surface-electrode ion traps*, Phys. Rev. A 78 (2008), 063410.

[62] M.G. House, *Analytic model for electrostatic fields in surface-electrode ion traps*, Phys. Rev. A 78 (2008), 033402.

[63] R. Schmied, *Electrostatics of gapped and finite surface electrodes*, New J. Phys. 12 (2010), 023038.

[64] V.K. Agarwal and V.K. Srivastava, *Thickness dependence of breakdown field in thin films*, Thin Solid Films 8 (1971), pp. 377–381.

[65] V.K. Agarwal and V.K. Srivastava, *Thickness dependent studies of dielectric breakdown in Langmuir thin molecular films*, Solid State Commun. 12 (1973), pp. 829–834.

[66] D. Mangalaraj, M. Radhakrishnan, and C. Balasubramanian, *Electrical conduction and breakdown properties of silicon nitride films*, J. Mater. Sci. 17 (1982), pp. 1474–1478.

[67] H.K. Kim and F.G. Shi, *Thickness dependent dielectric strength of a low-permittivity dielectric film*, IEEE Trans. Dielectrics Electric. Insulat. 8 (2001), pp. 248–252.

[68] H. Zhou, F. Shi, and B. Zhao, *Thickness dependent dielectric breakdown of PECVD low-k carbon doped silicon dioxide dielectric thin films: modeling and experiments*, Microelectron. J. 34 (2003), pp. 259–264.

[69] H. Bartzsch, D. Glöß, B. Böcher, P. Frach, and K. Goedicke, *Properties of SiO_2 and Al_2O_3 films for electrical insulation applications deposited by reactive pulse magnetron sputtering*, Surf. Coat. Technol. 174–175 (2003), pp. 774–778.

[70] J. Mueller, D. Pyle, I. Chakraborty, R. Ruiz, W. Tang, and R. Lawton, *Feasibility study of MEMS-based accelerator grid systems for micro-ion engines: Electric breakdown characteristics*, AIAA J. Propul. Power U.S.A. (1999).

[71] H.C. Miller, *Flashover of insulators in vacuum: review of the phenomena and techniques to improved holdoff voltage*, IEEE Trans. Electric. Insulat. 28 (1993), pp. 512–527.

[72] A.S. Pillai and R. Hackam, *Surface flashover of solid insulators in atmospheric air and in vacuum*, J. Appl. Phys. 58 (195), pp. 146–153.

[73] A.S. Pillai and R. Hackam, *Surface flashover of solid dielectric in vacuum*, J. Appl. Phys. 53 (1982), pp. 2983–2987.

[74] J.D. Kraus and D.A. Fleisch, *Electromagnetics with Applications*, 5th ed., McGraw-Hill Science/Engineering/Math, New York, 1999.

[75] D. İlbilge, C. Altindal, and M. Gökçen, *Frequency and gate voltage effects on the dielectric properties of Au/SiO2/n-Si structures*, Microelectron. Eng. 85 (2008), pp. 1910–1914.

[76] S.C. Thierauf, *High-speed circuit board signal integrity Artech House Publishers*, Norwood, MA, 2004.

[77] H. Johnson and M. Graham, *High Speed Signal Propagation: Advanced Black Magic* Prentice Hall, Upper Saddle River, NJ, 2003.

[78] P. Horowitz and W. Hill, *The Art of Electronics* Cambridge University Press, Cambridge, 1989.

[79] J. Krupka, J. Breeze, A. Centeno, N. Alford, T. Claussen, and L. Jensen, *Measurements of permittivity, dielectric loss tangent, and resistivity of float-zone silicon at microwave frequencies*, IEEE Trans. Microwave Theory Tech. 54 (2006), pp. 3995–4001.

[80] A. Tataroğlu, *Electrical and dielectric properties of MIS Schottky diodes at low temperatures*, Microelectron. Eng. 83 (2006), pp. 2551–2557.

[81] M.M. Bülbül, *Frequency and temperature dependent dielectric properties of Al/Si3N4/p-Si(100) MIS structure*, Microelectron. Eng. 84 (2007), pp. 124–128.

[82] S. Karataş, *Studies on electrical and the dielectric properties in MS structures*, J. Non-Crystalline Solid. 354 (2008), pp. 3606–3611.

[83] A.B. Selçuk, *On the dielectric characteristics of Au/SnO_2/n − Si capacitors*, Physica B 396 (2007), pp. 181–186.

[84] N. Tomozeiu, *Electrical conduction and dielectric relaxation of a − SiO_x $(0 < x < 2)$ thin films deposited by reactive RF magnetron sputtering*, Thin Solid Films 516 (2008), pp. 8199–8204.

[85] K.R. Brown, R.J. Clark, J. Labaziewicz, P. Richerme, D.R. Leibrandt, and I.L. Chuang, *Loading and characterization of a printed-circuit-board atomic ion trap*, Phys. Rev. A 75 (2007), 015401.

[86] C.E. Pearson, D.R. Leibrandt, W.S. Bakr, W.J. Mallard, K.R. Brown, and I.L. Chuang, *Experimental investigation of planar ion traps*, Phys. Rev. A 73 (2006), 032307.

[87] J.S. Chenard, C.Y. Chu, Z. Žilić, and M. Popović, *Design methodology for wireless nodes with printed antennas*, Proceedings of the 42nd Design Automation Conference, IEEE, Piscataway, NJ, 2005, pp. 291–296.

[88] M. Harlander, M. Brownnutt, W. Hänsel, and R. Blatt, *Trapped-ion probing of light-induced charging effects on dielectrics*, New J. Phys. 12 (2010), 093035.

[89] D.R. Leibrandt, R.J. Clark, J. Labaziewicz, P. Antohi, W. Bakr, K.R. Brown, and I.L. Chuang, *Laser ablation loading of a surface-electrode ion trap*, Phys. Rev. A. 76 (2007), 055403.

Downloaded by [University of Sussex Library] at 06:23 09 December 2011

[90] S.X. Wang, J. Labaziewicz, Y. Ge, R. Shewmon, and I.L. Chuang, *Individual addressing of ions using magnetic field gradients in a surface-electrode ion trap*, Appl. Phys. Lett. 94 (2009), 094103.

[91] S.X. Wang, Y. Ge, J. Labaziewicz, E. Dauler, K. Berggren, and I.L. Chuang, *Superconducting microfabricated ion traps*, Appl. Phys. Lett. 97 (2010), 244102.

[92] J. Labaziewicz, Y. Ge, P. Antohi, D. Leibrandt, K.R. Brown, and I.L. Chuang, *Suppression of heating rates in cryogenic surface-electrode ion traps*, Phys. Rev. Lett. 100 (2008), 013001.

[93] D. Stick, *Fabrication and characterization of semiconductor ion traps for quantum information processing*, Ph.D. thesis, University of Michigan, 2007.

[94] J. Labaziewicz, Y. Ge, D.R. Leibrandt, S.X. Wang, R. Shewmon, and I.L. Chuang, *Temperature dependence of electric field noise above gold surfaces*, Phys. Rev. Lett. 101 (2008), 180602.

[95] N. Daniilidis, T. Lee, R. Clark, S. Narayanan, and H. Häffner, *Wiring up trapped ions to study aspects of quantum information*, J. Phys. B 42 (2009), p. 154012.

[96] R.C. Sterling, H. Rattanasonti, S. Weidt, P. Srinivasan, K. Lake, A.H. Nizamani, M. Kraft, and W.K. Hensinger, *Two-dimensional ion trap arrays using silicon-on-insulator technology*, in preparation (2011).

[97] D. Stick, K.M. Fortier, R. Haltli, C. Highstrete, D.L. Moehring, C. Tigges, and M.G. Blain, *Demonstration of a microfabricated surface electrode ion trap*, preprint (2010). Available at arXiv:1008.0990v2.

[98] D. Leibrandt, J. Labaziewicz, R. Clark, I. Chuang, R. Epstein, C. Ospelkaus, J. Wesenberg, J. Bollinger, D. Leibfried, D. Wineland, D. Stick, J. Stick, C. Monroe, C.S. Pai, Y. Low, R. Frahm, and R. Slusher, *Demonstration of a scalable, multiplexed ion trap for quantum information processing*, Quantum Inf. Comput. 9 (2009), pp. 0901–0919.

[99] W.K. Hensinger, D. Stick, J. Sterk, M. Madsen, W. Noonan, M. Pedersen, S. Gross, M. Huff, and C. Monroe, *MEMS fabrication of silicon ion trap arrays*, Workshop on Trapped Ion Quantum Computing (Boulder, CO), 2006. Available at http://tf.nist.gov/ion/workshop2006/t11.pdf.

[100] M. Brownnutt, G. Wilpers, P. Gill, R.C. Thompson, and A.G. Sinclair, *Monolithic microfabricated ion trap chip design for scaleable quantum processors*, New. J. Phys. 8 (2006), p. 232.

[101] L. Deslauriers, S. Olmschenk, D. Stick, W.K. Hensinger, J. Sterk, and C. Monroe, *Scaling and suppression of anomalous heating in ion traps*, Phys. Rev. Lett. 97 (2006), 103007.

[102] Q.A. Turchette, Kielpinski, B.E. King, D. Leibfried, D.M. Meekhof, C.J. Myatt, M.A. Rowe, C.A. Sackett, C.S. Wood, W.M. Itano, C. Monroe, and D.J. Wineland, *Heating of trapped ions from the quantum ground state*, Phys. Rev. A 61 (2000), 063418.

[103] M.A. Rowe, A. Ben-Kish, B. DeMarco, D. Leibfried, V. Meyer, J. Beall, J. Britton, J. Hughes, W.M. Itano, B. Jelenkovic, C. Langer, T. Rosenband, and D.J. Wineland, *Transport of quantum states and separation of ions in a dual rf ion trap*, Quant. Inf. Comp. 2 (2002), pp. 257–271.

[104] S.A. Schulz, U. Poschinger, F. Ziesel, and F. Schmidt-Kaler, *Sideband cooling and coherent dynamics in a microchip multi-segmented ion trap*, New J. Phys. 10 (2008), p. 15.

[105] K. Mølmer and A. Sørensen, *Multiparticle entanglement of hot trapped ions*, Phys. Rev. Lett. 82 (1999), pp. 1835–1838.

[106] P.J. Lee, K.A. Brickman, L. Deslauriers, P.C. Haljan, L.M. Duan, and C. Monroe, *Phase control of trapped ion quantum gates*, J. Opt. B 7 (2005), pp. S371–S383.

[107] J.J. García-Ripoll, P. Zoller, and J.I. Cirac, *Speed Optimized Two-qubit gates with laser coherent control techniques for ion trap quantum computing*, Phys. Rev. Lett. 91 (2003), 157901.

[108] F. Diedrich, J.C. Bergquist, W.M. Itano, and D.J. Wineland, *Laser cooling to the zero-point energy of motion*, Phys. Rev. Lett. 62 (1989), pp. 403–406.

[109] R.G. DeVoe and C. Kurtsiefer, *Experimental study of anomalous heating and trap instabilities in a microscopic ^{137}Ba ion trap*, Phys. Rev. A 65 (2002), 063407.

[110] C. Roos, T. Zeiger, H. Rohde, H.C. Nägerl, J. Eschner, D. Leibfried, F. Schmidt-Kaler, and R. Blatt, *Quantum state engineering on an optical transition and decoherence in a paul trap*, Phys. Rev. Lett. 83 (1999), pp. 4713–4716.

[111] N. Daniilidis, S. Narayanan, S.A. Möller, R. Clark, T.E. Lee, P.J. Leek, A. Wallraff, S. Schulz, F. Schmidt-Kaler, and H. Häffner, *Fabrication and heating rate study of microscopic surface electrode ion traps*, New J. Phys. 13 (2011), p. 17.

[112] C. Tamm, D. Engelke, and V. Bühner, *Spectroscopy of the electric-quadrupole transition $^2S_{1/2}$ $(F = 0)$ $-^2D_{3/2}$ $(F = 2)$ in trapped $^{171}Yb^+$*, Phys. Rev. A 61 (2000), 053405.

[113] J. Britton, *Microfabrication techniques for trapped ion quantum information processing*, Ph.D. thesis, Univeristy of Colorado, Boulder, 2008, arXiv:1008.2222v1.

[114] R.J. Epstein, S. Seidelin, D. Leibfried, J.H. Wesenberg, J.J. Bollinger, J.M. Amini, R.B. Blakestad, J. Britton, J.P. Home, W.M. Itano, J.D. Jost, E. Knill, C. Langer, R. Ozeri, N. Shiga, and D.J. Wineland, *Simplified motional heating rate measurements of trapped ions*, Phys. Rev. A 76 (2007), 033411.

[115] V. Letchumanan, G. Wilpers, M. Brownnutt, P. Gill, and A.G. Sinclair, *Zero-point cooling and heating-rate measurements of a single $^{88}Sr^+$ ion*, Phys. Rev. A 75 (2007), 063425.